SQ52110

Current Sensing Comparator with Overcurrent Protection

General Description

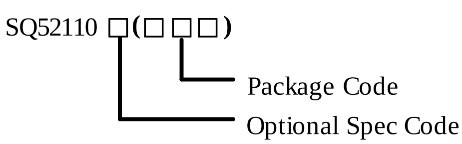
The SQ52110 is a current sensing comparator with overcurrent protection and used for the overcurrent protection applications.

It measures the voltage across a shunt resistor and compares this voltage with an adjustable threshold set by an external resistor. Independent of the supply voltage, the SQ52110 can handle the common voltage range between 0V and 36V and the differential input range from 0mV to 250mV.

An open drain alert output can be configured to operate in either a transparent mode where the output status follows the input state or in a latched mode where the alert output is cleared when the latch is cleared. The device response time setting is selectable, which enables overcurrent alerts to be issued in as fast as 10µs.

The SQ52110 operates from a single 2.7V to 5.5V supply, drawing a typical supply current of 135µA. It is specified over the extended operating temperature range of –40°C to +125°C, and is available in DFN2×2-10 and MSOP10 packages.

Ordering Information



Ordering Number	Package type	Note
SQ52110TDD	DFN2×2-10	
SQ52110FBP	MSOP10	

Features

- Wide Common Mode Range: 0V to 36V
- Selectable Response Times: 10µs, 50µs, 100µs
- Programmable Threshold:
  - Adjust Using Single Resistor
  - Programmable from 0 mV to 250 mV
- Accuracy:
  - Offset Voltage: ±500µV (Max)
  - Offset Voltage Drift: 0.5µV/°C (Max)
- Selectable Hysteresis: 2 mV, 4 mV, 8 mV
- Active Quiescent Current: 135µA (Typ)
- Selectable Disable Mode
  - Disabled Quiescent Current: 1.2µA (Max)
  - Disabled Input Bias Current: 500nA (Max)
- Open Drain Output with Latch Mode Available

Applications

- Overcurrent Protection
- Computers
- Servers
- Telecom Equipment
- Power Supplies
- Battery Chargers

Typical Application

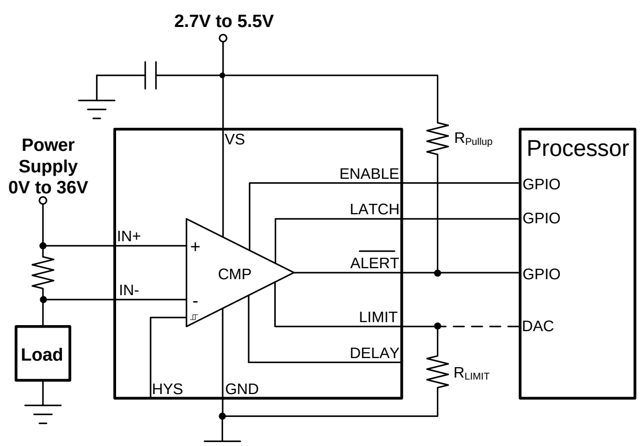
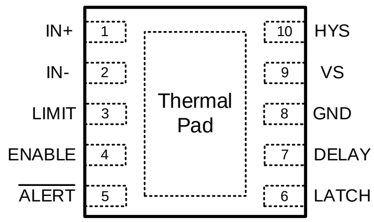
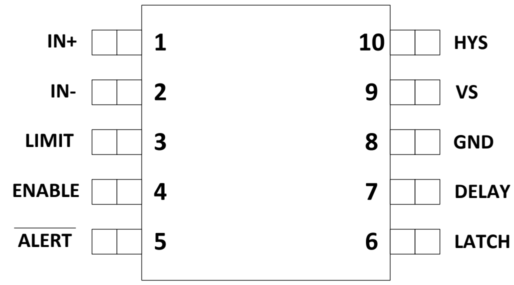


Figure 1. Typical Application

Pin out (Top View)





Part Number	Package type	Top Mark①
SQ52110TDD	DFN2×2-10	**W2*xyz***
SQ52110FBP	MSOP10	**EA*Axyz***

Note①： ***x=year code, y=week code, z= lot number code.***

Pin Number	Pin Name	Function Description
1	IN+	Connect to supply side of shunt resistor.
2	IN-	Connect to load side of shunt resistor.
3	LIMIT	Alert threshold limit input.
4	ENABLE	Enable or disable selection input.
5	$\overline{\text{ALERT}}$	Over-limit alert, active-low, open-drain output.
6	LATCH	Transparent or latch mode selection input.
7	DELAY	Response time selection input.
8	GND	Ground.
9	VS	Power supply, 2.7V to 5.5V.
10	HYS	Hysteresis setting input.
Thermal pad	DFN2×2-10 Only	This pad can be connected to ground or left floating.

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VS	-0.3	6	V
Differential V_{IN+} - V_{IN-}	-40	40	
Common mode, V_{IN+}, V_{IN-}	-0.3	40	
Alert output V_{ALERT}	-0.3	6	
Input voltage at Any Pin	-0.3	VS+0.3	
Junction Temperature, Operating	-40	150	°C
Storage Temperature	-65	150	
ESD: HBM (Human Body Model)	± 2000		V
ESD: CDM (Charged Device Model)	± 1000		V

Thermal Information

Parameter (Note 2)	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance(DFN2×2-10)	80	°C/W
θ_{JC} Junction-to-case Thermal Resistance(DFN2×2-10)	38	
P_D Power Dissipation T_A = 25°C(DFN2×2-10)	1.2	W
θ_{JA} Junction-to-ambient Thermal Resistance(MSOP10)	75	°C/W
θ_{JC} Junction-to-case Thermal Resistance(MSOP10)	37	
P_D Power Dissipation T_A = 25°C(MSOP10)	1.3	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Differential V_{IN+} - V_{IN-}	0	250	mV
VCC	2.7	5.5	V
Common mode, V_{IN+}, V_{IN-}	0	36	
Junction Temperature Range	-40	125	°C

Electrical Characteristics

At T_A=25°C, V_{IN}=V_{IN+}–$V_{IN–}$=0mV, V_S=3.3V, V_{IN+}=12V, V_{LIMIT}=10mV, and DELAY=100µs, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input						
Common Mode Input Voltage	V_{CM}		0		36	V
Differential Input Voltage	V_{IN}	V_{IN}=V_{IN+}-V_{IN-}	0		250	mV
Common Mode Rejection	CMR	V_{IN}=0V~36V, T_A=-40°C~+125°C	110	120		dB
Offset Voltage, RTI	V_{OS}	V_S=3.3V, DELAY=100µs		-75	-500	µV
		V_S=3.3V, DELAY=50µs		-125	-500	
		V_S=3.3V, DELAY=10µs		-350	-650	
Offset Voltage Drift, RTI	dV_{OS}/dT	T_A=-40°C~+125°C		0.1	0.5	µV/°C
Power Supply Rejection Ratio	PSR	V_S=2.7V~5.5V, V_{IN+}=12V, T_A=-40°C~+125°C		5	60	µV/V
Input Bias Current (Note 3)	I_B			3.5	8	µA
		Disable mode		0.05	0.5	
Input Offset Current (Note 4)	I_{OS}			±0.1		µA
Limit Threshold Output Current	I_{LIMIT}	T_A=25°C	19.85	20	20.15	µA
		T_A=-40°C~+125°C	19.8		20.2	
Digital Input / Output						
Alert Propagation Delay	t_p	Delay=open, overdrive=1mV (Note 5)		10		µs
		Delay=GND, overdrive=1mV		50		
		Delay=VS, overdrive=1mV		100		
Hysteresis	HYS	HYS=open		2		mV
		HYS=GND		4		
		HYS=VS		8		
High Level Input Voltage	V_{IH}	Latch, enable	1.4		6	V
		Delay, hysteresis	V_S-0.5		6	
Low Level Input Voltage	V_{IL}	Latch, enable	0		0.4	V
		Delay, hysteresis	0		0.5	
Alert Low Level Output Voltage	V_{OL}	I_{OL}=3mA		50	100	mV
$\overline{\text{ALERT}}$ Terminal Leakage Input Current		V_{OH}=3.3V		0.1	1	µA
Digital Leakage Input Current		Pin ENABLE, LATCH, DELAY and HYS, 0<V_{IN}<V_S		1	2	µA
Power Supply						
Quiescent Current	I_Q	V_{IN}=0mV, T_A=-40°C~+125°C		135	155	µA
		V_{IN}=0mV, disable mode, HYS=2mV		0.6	1.2	
Timing Requirements						
Start-up Time				1		ms
Enable Time	t_{en}			150		µs
Disable Time	t_{dis}			20		µs

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2: θ_{JA} is measured under natural convection at T_A =25°C and chip mounted on low-effective four-layer thermal conductivity test board
Note 3: Input bias current is decided by the average of the input currents of the pin IN+ and IN-.
Note 4: Input offset current is decided by the error between the input currents of the pin IN+ and IN-.
Note 5: Overdrive = V_{IN} – V_{LIMIT}.

Application Information

Operation

The SQ52110 is a 36V, common mode comparator designed specifically for overcurrent protection applications. To reduce system component count, this device combines both the current sensing amplifier and threshold comparison into a single product for the overcurrent detection function. Programming this comparison threshold is configured through a single external resistor, thus simplifying the circuit design while allowing for easy adjustments to the threshold when needed. The value of the threshold setting resistor is selected based on an internal 20μA current source to achieve a corresponding signal to the voltage developed across the current sensing resistor in series with the load current being monitored.

The device is designed to accommodate a wide range of application requirements, including common mode voltage, noise thresholds and signal ranges. A wide signal threshold range reaching up to 250mV is available to accommodate both power sensitive applications requiring small dissipations across a current sensing resistor and larger current sensing resistors used in lower current applications.

Additional features available with the SQ52110 include a disable mode for reducing the current consumption of the device to below 10μA, an output mode selector to enable a latched or a transparent alert output, and a selectable hysteresis value and alert response delay.

The wide signal range of the device is further enhanced with an adjustable hysteresis value to adjust the characteristics of the comparator, thus allowing for better accommodation of the full input range. The selectable alert response delays present in the SQ52110 assist in optimizing device operation to account for the system noise levels and operating characteristics required from this device. Longer delay settings allow for added rejection of system noise commonly present, thus reducing the potential for false alerts resulting from noise spikes that can easily occur in high speed comparators.

Current Limit Threshold Setting

The device will determine if an overcurrent event is present by comparing the measured differential voltage developed across the current sensing resistor to the corresponding signal programmed at the LIMIT terminal. The threshold voltage for the LIMIT terminal can be set using a resistor or an external voltage source.

Resistor Controlled Current Limit

The typical approach for setting the limit threshold voltage is to connect a resistor from the LIMIT terminal to ground. The value of this resistor R_{LIMIT} is chosen in order to create a corresponding voltage at the LIMIT terminal equivalent to the voltage developed by the load current flowing through the current sensing resistor. An internal 20μA current source is present at the LIMIT terminal that creates the corresponding voltage depending on the value of R_{LIMIT}.

Voltage Source Controlled Current Limit

The second method for setting the limit voltage is to connect the LIMIT terminal to a programmable DAC or other external voltage source. The benefit of this method is the ability to adjust the current limit to account for different threshold voltages that are used for different system operating conditions. For example, this method can be used in a system that has one current-limit threshold level that must be monitored during the power-up sequence but different thresholds must be monitored during other system operating modes.

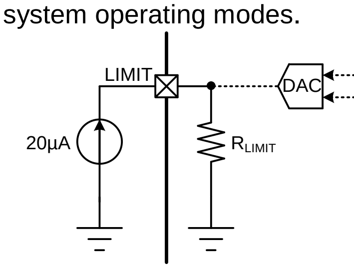


Figure 2. Voltage Source Controlled Current Limit

Delay Setting

The device response time for overcurrent events is adjustable based on the DELAY terminal setting. Three response time settings are available, ranging from 10μs to 100μs. The primary purpose for the three different delay settings is to offer a trade-off between a faster alert response and a more precise overcurrent threshold level detection.

The device has a 10μs internal comparison window. This single comparison window is the fundamental time unit used for all three delay settings. For the 10μs delay setting, the device compares the average of the input signal during the 10μs comparison window to the threshold limit programmed at the LIMIT terminal. If the averaged input signal exceeds the threshold at the end of the 10μs comparison window, the output alert will trigger and pull the $\overline{\text{ALERT}}$ terminal low. However, if the averaged input does not exceed the threshold at the end of the 10μs comparison window, there will be no change in the output alert status, which remains high to indicate that no overcurrent event is detected.

For the 50μs delay setting, there is a counter. For the 10μs internal comparison window, if the average input signal exceeds the threshold limit, counter will plus one;

if the average input signal does not exceed the threshold limit, counter minus one. When the counter have reached five overcurrent comparisons, the output alert will trigger and pull the $\overline{\text{ALERT}}$ terminal low. After the $\overline{\text{ALERT}}$ terminal is pulled low, once any single 10μs comparison window fails to detect an overcurrent condition, the internal counter will reset and pull the $\overline{\text{ALERT}}$ terminal high.

The 100μs delay setting operates in the same manner as the 50μs method, but instead requires the counter having reached ten overcurrent comparisons with an input signal exceeding the threshold limit in order to issue an output alert and pull the $\overline{\text{ALERT}}$ terminal low.

Requiring multiple consecutive overcurrent detections aides significantly in reducing the likelihood of system noise causing false alerts, which can be extremely detrimental to critical system operations. However, by enabling an alert window equal to the comparison window of 10μs, the device still has the flexibility to be used in fast overcurrent detection applications that require quick responses to rapidly changing system operating characteristics.

In Figure 3, the device alert output response is shown for both a 10μs delay setting and a 50μs delay setting based on the same input signal condition.

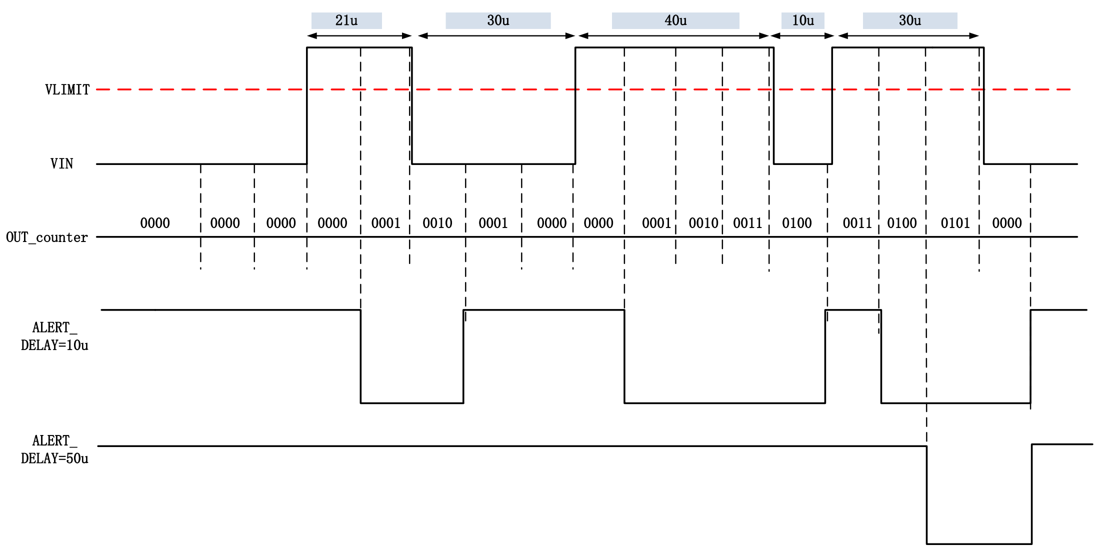


Figure 3. DELAY Terminal Settings

As discussed previously, there are three different available delay settings that are configured based on the signal connected to the DELAY terminal. As shown in figure 4. The DELAY terminal must be either connected directly to ground, directly to supply, or left completely floating. Additional external resistors should not be connected to this terminal. If a resistance is required by the application to be placed in series with either the supply or ground connection to the DELAY terminal, this resistance must be limited to 1kΩ so as to not conflict with the internal level-detection circuitry.

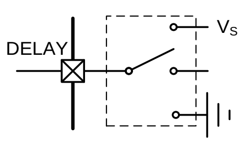


Figure 4. Delay Response

DELAY Pin	$\overline{\text{ALERT}}$ Delay Time (us)
Open or floating	10
GND	50
V_S	100

Hysteresis Setting

Device hysteresis is adjustable based on the setting at the hysteresis (HYS) terminal. The smallest setting for hysteresis on the device (2mV) is enabled by leaving the HYS terminal open and floating. A 4mV hysteresis is set by connecting the HYS terminal to ground; connecting this terminal to the supply voltage sets the hysteresis to 8mV, as shown in Figure 5. The HYS terminal must be either connected directly to ground, directly to supply, or left completely floating. Additional external resistors should not be connected to this terminal. If a resistance is required by the application to be placed in series with either the supply or ground connections to the HYS terminal, this resistance must be limited to 1kΩ so as to not conflict with the internal level-detection circuitry.

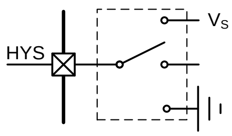


Figure 5. HYS Response

The very wide dynamic input range of the SQ52110 necessitates an adjustable hysteresis to ensure that the device can be more appropriately configured based on the specific operating conditions and requirements of the application. Figure 6 illustrates the transition locations for the $\overline{ALERT}$ terminal based on where the input signal V_{IN} is measured relative the limit threshold V_{LIMIT}. The corresponding hysteresis levels and physical terminal settings for the device are shown in table.

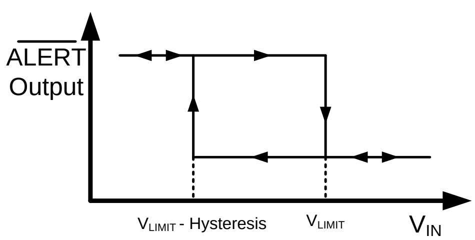


Figure 6. Typical Comparator Hysteresis

HYS Pin	Hysteresis Threshold (mV)
Open or floating	2
GND	4
V_S	8

Alert Output

The device $\overline{ALERT}$ terminal is an active low, open drain output. This output is designed to be pulled low when the input conditions are detected to be out of range. This open drain output pin is recommended to include a 10kΩ, pull-up resistor to the supply voltage. This open drain terminal can be pulled up to a voltage beyond the supply voltage V_S, but should not exceed 5.5 V.

Alert Mode

The device has two output operating modes that are selected based on the LATCH terminal setting. The two operating modes are transparent mode and latch mode. These modes change how the $\overline{ALERT}$ terminal responds to the changing input signal conditions.

Transparent Output Mode

The device is set to transparent mode when the LATCH terminal is pulled low, thus allowing the output alert state to change and follow the input signal with respect to the programmed alert threshold. For example, when the differential input signal rises above the alert threshold, the alert output terminal will be pulled low. As soon as the differential input signal drops below the alert threshold for 10μs, the output will return to the default high output state.

A common implementation using the device in transparent mode is to connect the $\overline{ALERT}$ terminal to a hardware interrupt input on a controller. As soon as an overcurrent condition is detected in the device and the $\overline{ALERT}$ terminal will be pulled low, the controller interrupt terminal will detect the output state change and can begin making changes to the system operation needed to address the overcurrent condition.

Latch Output Mode

Some applications do not have the functionality available to continuously monitor the state of the output $\overline{ALERT}$ terminal to detect an overcurrent condition.

Latch mode is specifically intended to accommodate these applications. As shown in table, the device is placed in latch mode by setting the voltage on the LATCH terminal to a logic high level. In latch mode, when an overlimit condition is detected and the $\overline{ALERT}$ terminal is pulled low, the $\overline{ALERT}$ terminal will not return to the default high level when the differential input signal drops below the alert threshold level for 10μs. In order to clear the alert, the LATCH terminal must be pulled low for at least 20μs. Pulling the LATCH terminal low allows the $\overline{ALERT}$ terminal to return to the default high level provided that the differential input signal has dropped below the alert threshold. If the input signal is still above the threshold limit when the LATCH terminal is pulled low, the $\overline{ALERT}$ terminal will remain low. When the alert condition is detected by the system controller, the LATCH terminal can be set back to high in order to place the device back in latch mode.

The difference between latch mode and transparent mode is how the alert output will respond when an overcurrent event ends. In transparent mode, when the differential input signal drops below the limit threshold level for 10µs, the output state will return to the default high setting to indicate that the overcurrent event had ended.

Output Mode	Latch Terminal Setting
Transparent mode	LATCH = low
Latch mode	LATCH = high

The latch and transparent modes are represented in Figure 7. In this figure, when V_{IN} drops back below the V_{LIMIT} threshold for the first time, the LATCH terminal will be pulled high. With the LATCH terminal pulled high, the device is set to latch mode so that the alert output state will not return high when the input signal drops below the V_{LIMIT} threshold. Only when the LATCH terminal is pulled low, the $\overline{ALERT}$ terminal will return to the default high level, thus indicating the input signal is below the limit threshold. When the input signal drops below the limit threshold for the second time, the LATCH terminal will already be pulled low. The device is set to transparent mode at this point and the $\overline{ALERT}$ terminal is pulled back high as soon as the input signal drops below the alert threshold.

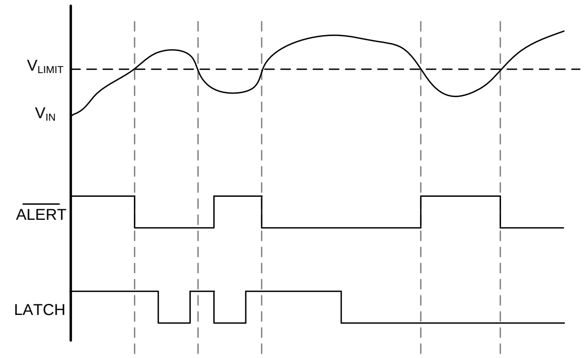


Figure 7. Transparent versus Latch Mode

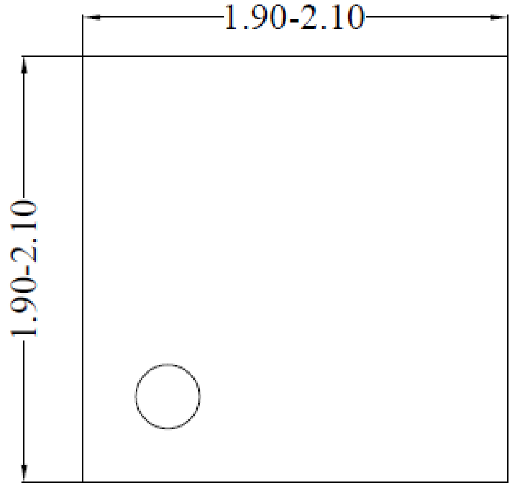
Disable Mode

The SQ52110 has an ENABLE terminal that allows the device to be placed into an active enabled state or a low power disabled state where a total of less than 10µA is consumed from all terminals. This disable state allows the device to be used in applications where very low current consumption is required to extend battery life where constant monitoring is not required.

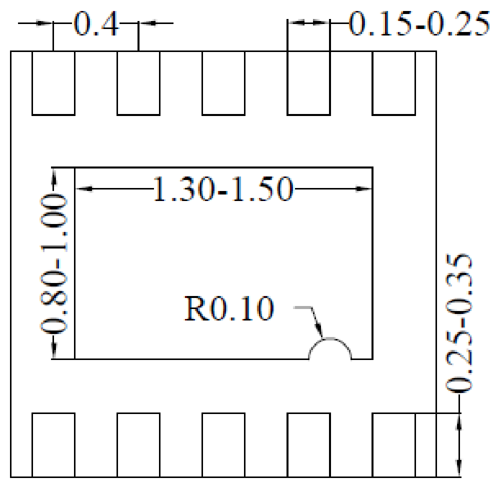
The device will require approximately 20µs to enter the low power state when the ENABLE terminal transitions from high to low, as shown in table. To return to the enabled active state, the device will require approximately 300µs to return to normal operation when the ENABLE terminal transitions from low to high, thus taking the device out of the low power state.

Enable Mode	ENABLE Terminal Setting
Disable mode	ENABLE = low
Enable mode	ENABLE = high

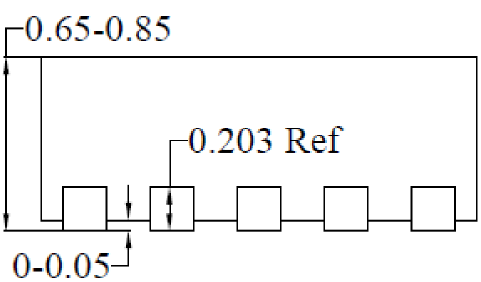
DFN2x2-10 Package Outline Drawing



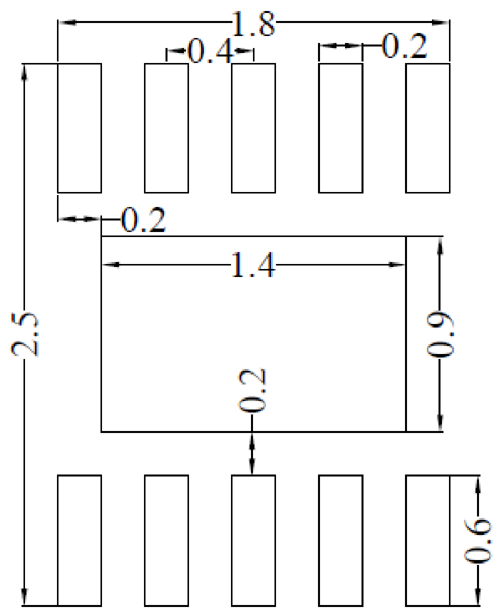
Top View



Bottom view



Bottom View

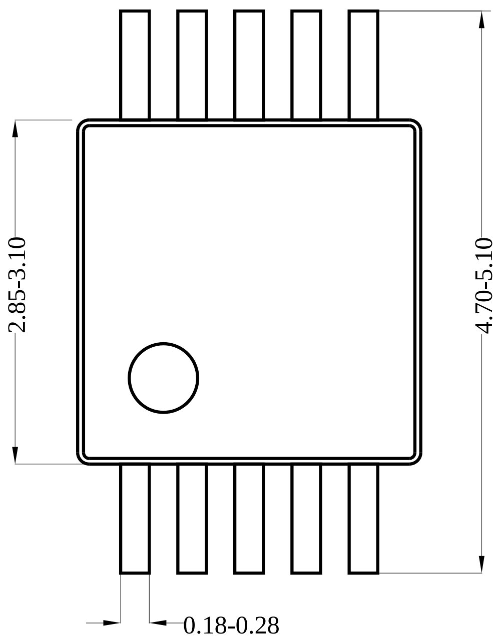


Recommended PCB layout

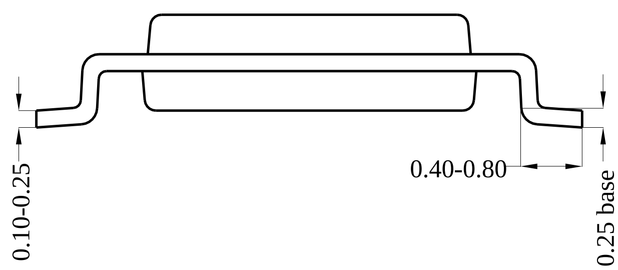
(Only for reference)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr.

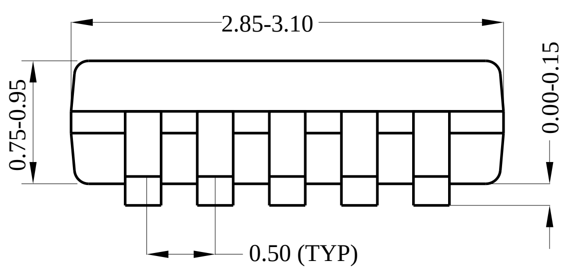
MSO10 Package outline & PCB layout



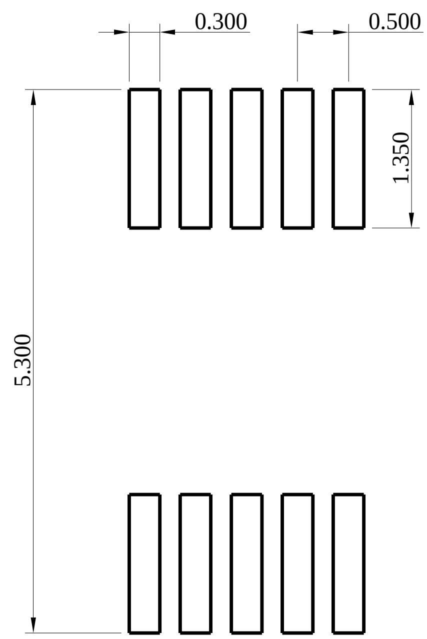
Top view



Side view



Front view



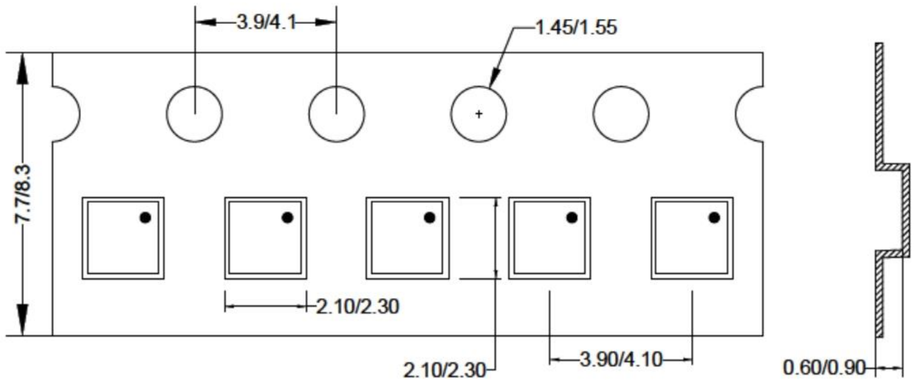
Recommended Pad Layout

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

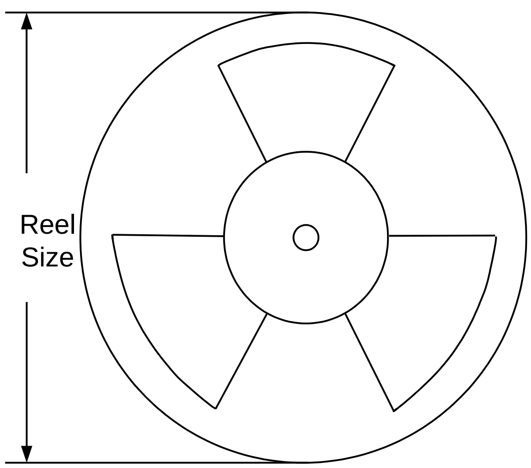
1. Taping orientation

DFN2x2-10



Feeding direction →

2. Carrier Tape & Reel specification for packages



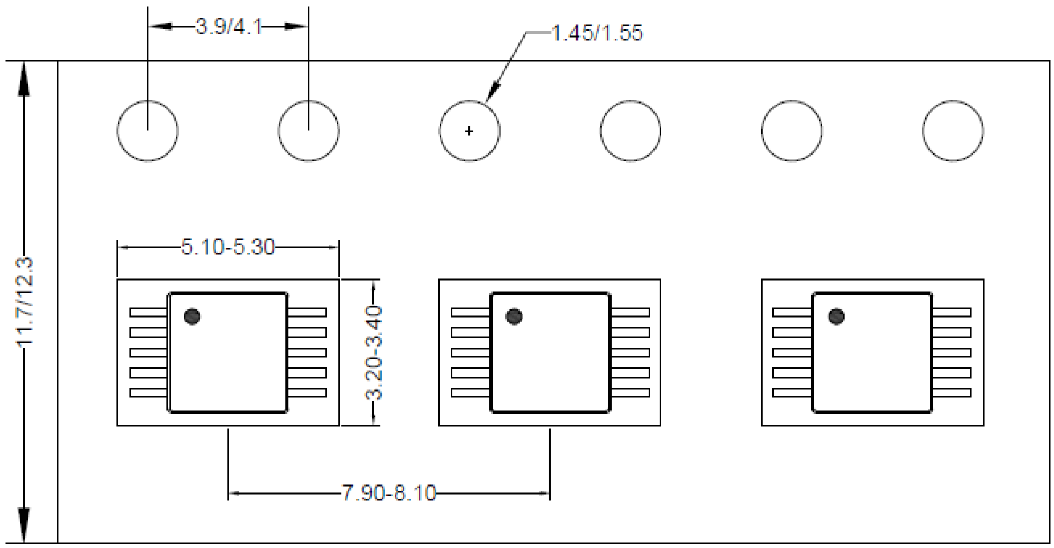
Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2x2-10	8	4	7"	400	160	3000

3. Others: NA

Taping & Reel Specification

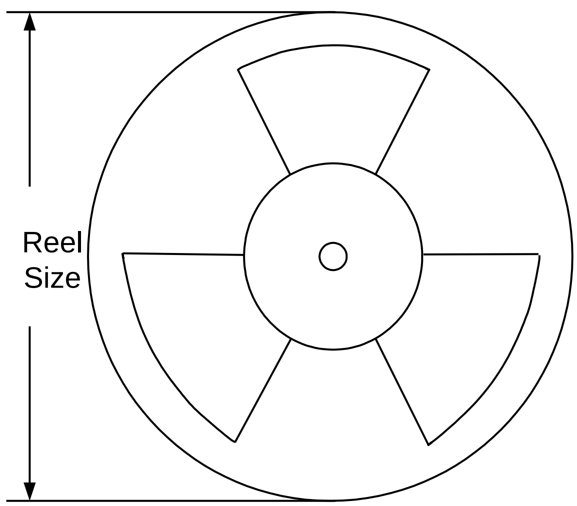
1. Taping Orientation

MSOP10



Feeding direction

2. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
MSOP10	12	8	13"	400	400	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Oct.9, 2021	Revision 0.9	Initial Release
Apr.8, 2022	Revision 0.9A	Update the taping orientation in Taping & Reel Specification
July 17, 2023	Revision 0.9B	Add new package MSOP10.
July 17, 2024	Revision 1.0	Production Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. **Applications.** Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com