SY5601A

IEEE 802.3 af/at PoE-Compliant Powered Device (PD) Controller

General Description

The SY5601A is an IEEE 802.3 af/at PoE-compliant Powered Device (PD) controller. It features detection and classification modes and a 100V-rated pass switch. Built-in thermal protection accommodates transient and overload conditions by shutting down the pass switch to protect the input source. Inrush current limiting is included to gradually charge the downstream input capacitor without interruption due to die heating.

The SY5601A can automatically generate a pulsed voltage to maintain the PSE power when the downstream DC/DC converter operates in light or no-load mode. The AMPS current amplitude is programmable through an external resistor.

Features

- Fully Compatible with 802.3af/at Specifications
- 100V, 0.45Ω Integrated PASS Switch
- 900mA Normal Operation Current Limit
- 100mA Inrush Current Limit
- Auto-Maintain Power Signature
- Open Drain Power Good Output
- SO8E Package

Applications

- VoIP Telephones
- Network Cards
- Security Camera Systems
- Safety Backup Power
- Remote Internet Power

Typical Application

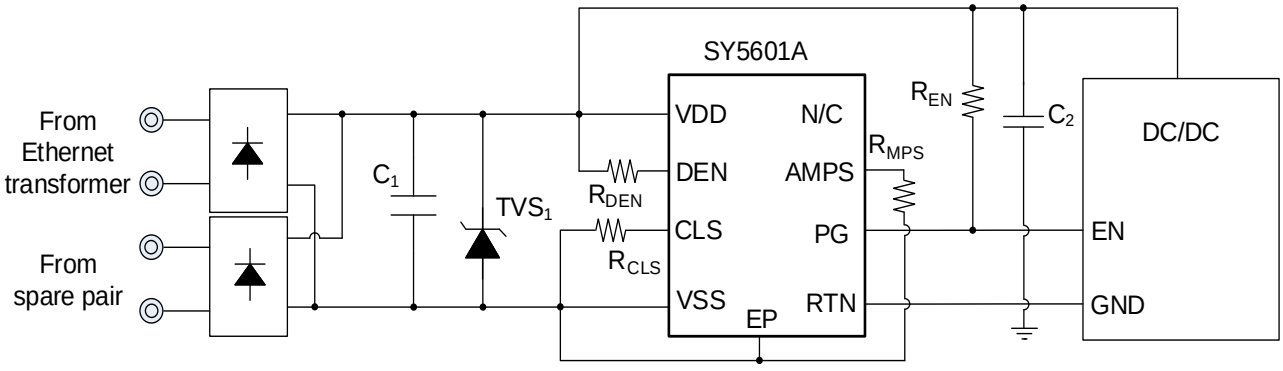


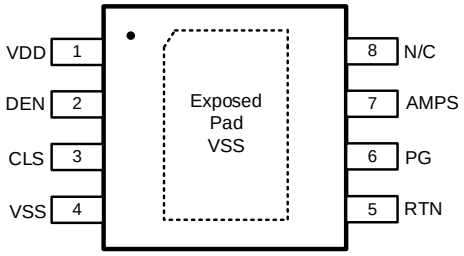
Figure 1. Schematic Diagram

Ordering Information

Ordering Number	Package Type	Top Mark
SY5601AFCP	SO8E	**AAFD*xyz***

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Description

Pin Number	Pin Name	Pin Description
1	VDD	Positive power supply terminal for PoE input.
2	DEN	Detection. Connect a 24.9kΩ resistor between VDD and DEN for PoE detection.
3	CLS	Classification. Connect a resistor from CLS to VSS to program the classification current.
4, EP	VSS	Negative power supply terminal from PoE input.
5	RTN	Drain of PD pass switch and negative rail input of the DC/DC converter.
6	PG	Power Good Indicator. Active low, open-drain converter disable output, referenced to RTN.
7	AMPS	Auto-maintain power signature pin. Connect a resistor between this pin and VSS to program the AMPS current. Leave open to disable the function.
8	N/C	Not connected internally.

Block Diagram

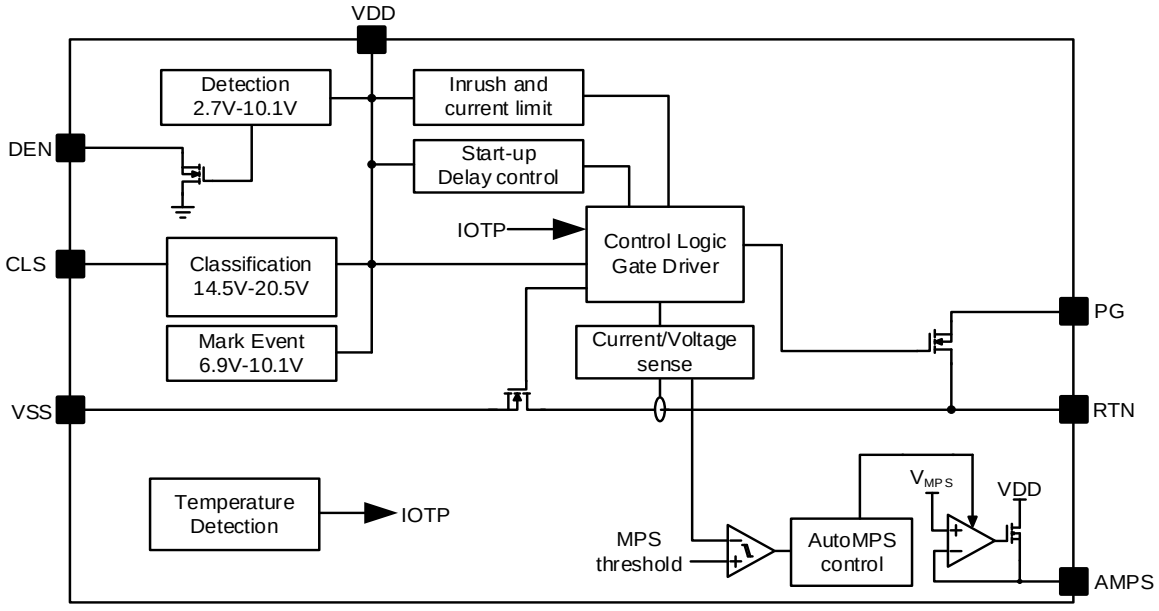


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)		Min	Max	Unit
Pin Voltage in Respect to VSS				
VDD		-0.3	100	V
DEN,RTN,PG		-0.3	VDD+0.7	
CLS, AMPS (Note 6)		-0.3	5.5	
Pin Voltage in Respect to RTN				
VDD, PG		-0.3	100	V
Pin Current				
PG Sink Current (Note 3)			0.5	mA
Junction Temperature, operating		-45	150	°C
Lead Temperature (Soldering, 10 sec.)			260	
Storage Temperature		-65	150	
V_{ESD} Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001-2023		±2000	V
	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002-2022		±500	

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA}, Junction-to-Ambient Thermal Resistance		35	℃/W
θ_{JC}, Junction-to-Case Thermal Resistance		24	
θ_{JB}, Junction-to-Board Thermal Resistance		9	
PD Power Dissipation T_A = 25°C		2.8	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Supply Voltage VDD	0	57	V
Maximum PG Sink Current		0.1	mA
Maximum AMPS Source Current		13	mA
Operating Junction Temperature (T_J)	-40	125	℃

Electrical Characteristics

(VDD, CLS, DEN, and RTN voltages are referenced to VSS, and PG voltage is referenced to RTN. VDD-VSS=48V, R_{DEN}=24.9 kΩ, R_{CLS}=90.9 Ω, T_J=-40℃ to +125℃, typical values are tested at T_J=25℃ unless otherwise noted. (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Detection	Detection On	V_{DET_ON}	V_{DD} rising	0.6	1	1.4	V
	Detection Off	V_{DET_OFF}	V_{DD} rising	9.8	11	12.2	V
	DEN Leakage Current	V_{DET_LK}	V_{DET}=V_{DD} =57V, measure I_{DET}		0.1	5	μA
	Bias Current		V_{DD} =10.1V, float DEN pin, not in Mark event, measure I_{SUPPLY}			12	μA
	Detection Current	I_{DET}	V_{DD}=1.4V, measure I_{SUPPLY}	53.8	55.6	58.3	μA
			V_{DD}=10.1V, measure I_{SUPPLY}	395	410	425	μA
Classification	Classification Stability Time		(Note 5)		90		μs
	V_{CLASS} Output Voltage	V_{CLASS}	13V<VDD<21V, 1mA<I_{CLASS}<42mA	2.37	2.5	2.63	V
	Classification Current	I_{CLASS}	13 V ≤ V_{DD}≤ 21V, Guaranteed by V_{CLASS}				
			R_{CLASS} =1270Ω, 13V ≤ V_{DD}≤ 21V	1.8	2	2.4	mA
			R_{CLASS} = 243Ω, 13V ≤ V_{DD}≤ 21V	9.9	10.55	11.3	
			R_{CLASS} = 137Ω, 13V ≤ V_{DD}≤ 21V	17.7	18.7	19.8	
			R_{CLASS} = 90.9Ω, 13V ≤ V_{DD}≤ 21V	26.6	28.15	29.7	
			R_{CLASS} =63.4 Ω, 13V ≤ V_{DD}≤ 21V	38.2	40.4	42.6	
	Classification Lower Threshold	V_{CL_ON}	V_{DD} rising, class regulator turns on	11	12	13	V
	Classification Upper Threshold	V_{CL_OFF}	V_{DD} rising, class regulator turns off	21	22	23	
	Classification Hysteresis	V_{CL_H}	Low side hysteresis	0.4	0.94	1.5	
			High side hysteresis	0.2	0.49	0.9	
	Mark Event Reset Threshold	V_{MARK_L}		4	5	6	V
	Max Mark Event Voltage	V_{MARK_H}		11	12	13	V
	Mark Event Resistance	R_{MARK}	2-point measurement at 7V and 10V	5	9	13	kΩ
	Device Supply Current During Classification	I_{IN_CLASS}	V_{DD}=17.5V, CLASS floating	110	190	270	μA
	Class Leakage Current	I_{LK}	V_{DD}=57V, V_{CLASS}=0V			1	μA
PD UVLO	VDD Turn on Threshold	$V_{DD\_VSS\_R}$	V_{DD} rising	33	35	37	V
	VDD Turn off Threshold	$V_{DD\_VSS\_F}$	V_{DD} falling	29	31	33	V
	VDD UVLO Hysteresis	$V_{DD\_VSS\_HYS}$		3.2	4.2	5.2	V
	Device Supply Current During Operation	I_{IN}		240	360	480	μA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
PG	ON Resistance	R_{DS-PG}	I_{PG} = 0.5mA	1.5	2.7	5.5	kΩ
	Output High Leakage Current		V_{PG}=48V			1	μA
PASS device and current limit	ON Resistance	R_{DS-RTN}	I_{RTN}=100mA	0.2	0.41	0.8	Ω
	Leakage Current	I_{RTN-LK}	V_{DD}=V_{RTN}=57V		1	15	μA
	Current Limit	I_{LIMIT}	V_{RTN}=1V	750	900	1050	mA
	Inrush Current Limit	I_{INRUSH}	V_{RTN}=2V	45	106	175	mA
	Inrush Current Termination		V_{RTN} falling	1.1	1.2	1.3	V
	Inrush to Operation Mode Delay	T_{DELAY}		80	100	120	ms
	Current Fold-Back Threshold		V_{RTN} rising		10.5		V
	Fold-Back Deglitch Time		V_{RTN} rising to inrush current fold-back		1.1		ms
AMPS	MPS DC Supply Current		Startup has completed, I_{RTN} = 0 mA			0.8	mA
	Auto MPS Pulsed Voltage		Startup has completed, I_{RTN}<15 mA, R_{MPS} ≥160Ω	2.37	2.5	2.63	V
	Automatic MPS Falling Current Threshold		Startup has completed, and the I_{RTN} falling threshold will generate MPS pulses		29		mA
			Hysteresis on RTN current		3		mA
	POE MPS Time High			85	106	125	ms
	POE MPS Time Low			170	216	265	ms
Protection	Thermal Shutdown Temperature (Note 5)	T_{SD}			150		℃
	Thermal Shutdown Hysteresis (Note 5)	T_{HYS}			20		℃

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured with natural convection at T_A = 25°C on a 1oz two-layer Silergy evaluation board. Case temperature θ_{JC} is measured at pin 4 or pin 5.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \backsimeq T_J$ = 25℃. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

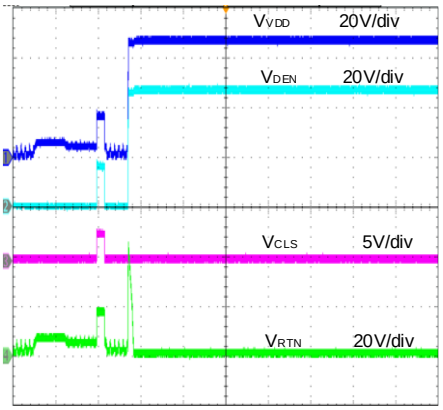
Note 5: Guaranteed by design or statistical correlation and not production tested.

Note 6: Voltage should not be externally applied to this pin.

Typical Performance Characteristics

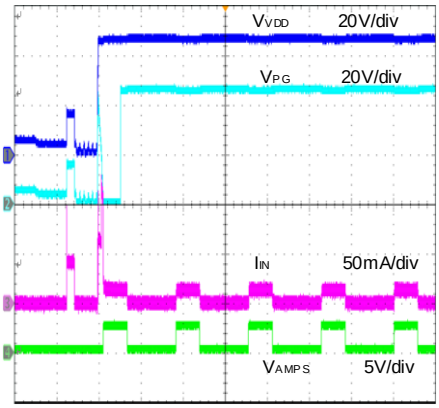
(Test conditions: PSE input before the bridge rectifiers, there is no load between VDD and RTN, ambient temperature: 25±5℃.)

af PSE Operation Test



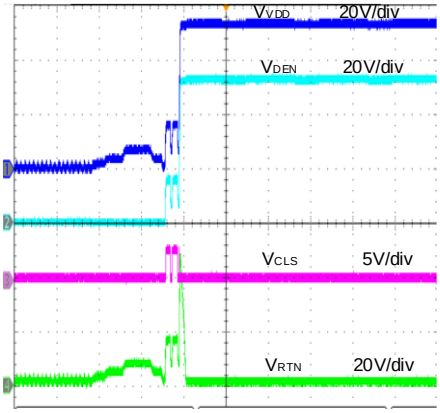
Time (200ms/div)

af PSE Operation Test



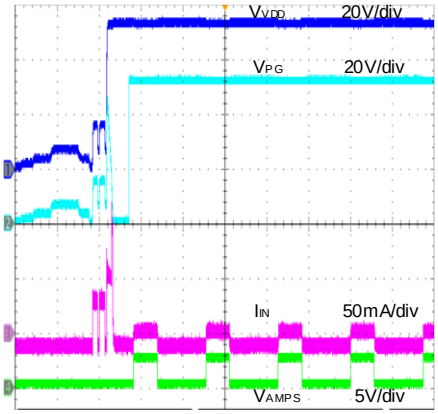
Time (200ms/div)

at PSE Operation Test



Time (200ms/div)

at PSE Operation Test



Time (200ms/div)

Detailed Description

DEN Detection and Enable

The DEN pin implements two functions:

1. A resistor placed between VDD and DEN produces a detection signature when the voltage difference between VDD and VSS is approximately 1.4V to 10.9V. Outside this range, the controller disconnects the resistor to conserve power. According to the IEEE 802.3af/at standard, the detection signature resistance (R_{DEN}) should be between 23.75kΩ to 26.25kΩ, or 25kΩ ± 5%. An R_{DEN} resistor value of 24.9 kΩ ± 1% is recommended for all applications.
2. Pulling DEN down to VSS during powered operation turns the internal PASS Switch and class regulator off. The falling threshold to disable the PASS Switch is 3.7V, with a debounce time of 3ms to prevent false triggers during surge tests.

Classification

In the classification mode, the PSE classifies the PD into one of five power levels or classes, enabling efficient power distribution. The classes are detailed in Table 1, which defines the class the PD must advertise. An external resistor (R_{CLS}) connected from CLS to VSS sets the classification current. The PSE may disconnect a PD if it draws more power than its stated class power.

During hardware classification, the PSE presents a fixed voltage between 15.5V and 20.5V to the PD, drawing a fixed current set by R_{CLS}. The PSE measures PD current to determine which available classes are advertised (see Table 1). The SY5601A disables classification when the input voltage exceeds 22V to avoid excessive power dissipation.

Table 1. Class Resistor Selection

Class	Power at PD(W)	Class Current (mA)	Resistor (Ω)
0	0.44~12.95	0~4	1270
1	0.44~3.84	9~12	243
2	3.84~6.49	17~20	137
3	6.49~12.95	26~30	90.9
4	12.95~25.5	36~44	63.4

2-Event Classification

The SY5601A can be used as a Type-1 PD supporting classes 0-3, as shown in Table 1. It also distinguishes class 4 with a 2-event classification.

In 2-event classification, the Type-2 PSE reads the power classification twice. Figure 2 shows an example of a 2-event classification. The first classification event occurs when the PSE presents a voltage between 14.5V to 20.5V to the SY5601A, and the SY5601A presents a class-4 load current. The PSE then drops the input voltage to the mark voltage range of 6.9V to 10.1V, signaling the first mark event. The SY5601A presents a load current between 0.5mA and 2mA in the mark event voltage range.

The PSE repeats this sequence, signaling the second classification and second mark event. The PSE then applies power to the SY5601A, which charges the DC/DC input capacitor with a controlled inrush current.

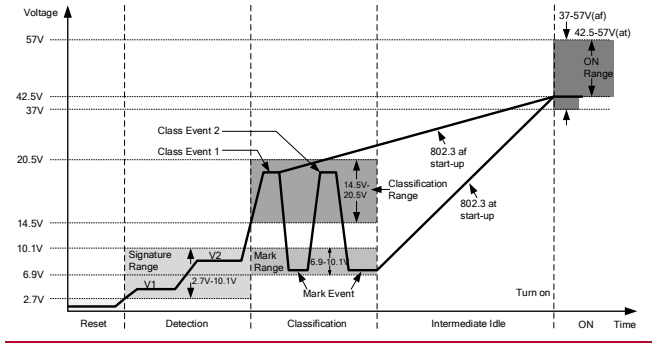


Figure 3. PD Interface Operation Description

PD Interface UVLO and Inrush Current Limit

When PD is powered by PSE and VDD exceeds the turn-on threshold, the hot-swap switch begins passing a limited current (I_{INRUSH}) to charge the downstream DC/DC converter's input capacitor. The startup charging current I_{INRUSH} is limited to around 100mA to comply with the IEEE 802.3af/at standard.

If V_{RTN} drops below 1.2V, and the 100ms inrush delay from UVLO initiation is complete, the current limit of the pass switch changes to 900mA. Simultaneously, the SY5601A releases the PG signal, which rises high if pulled up externally, allowing PG to enable the DC/DC controller. If V_{VDD} drops below the falling UVLO threshold, the pass switch MOSFET is disabled.

If an output current overload occurs on the internal pass switch, the current limit activates, causing V_{RTN}-V_{VSS} to rise. If V_{RTN} exceeds 10.5V for more than 1.1ms, the current limit reverts to the inrush value, and PG is pulled down simultaneously.

Figure 4 illustrates the current limit and PG logic during startup from the PSE power supply.

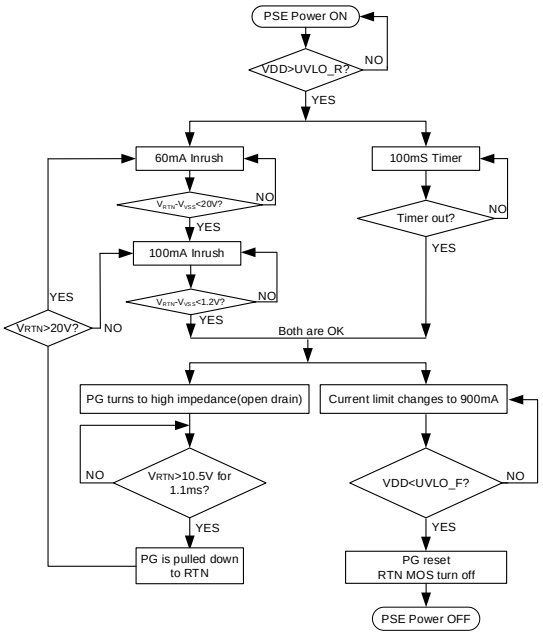


Figure 4. Typical Startup Sequence of PoE Input

PG Control (PG)

When the input voltage exceeds UVLO, the SY5601A initiates inrush current, and a 100ms timer starts. PG is pulled down to RTN until the pass switch turns on and the 100ms timer expires. It remains in a high impedance state at all other times. This pin is an open-drain output and may require a pull-up resistor or other interface to the downstream load. PG may be left open if not used.

Auto-Maintain Power Signature

Maintain power signature is an electrical signature generated by the PD to indicate to the PSE that it remains connected after the operating voltage is applied. For a Type 1 or Type 2 PD, a valid power signature consists of a minimum DC current of 10mA or a 10mA pulsed current for at least 75ms every 325ms.

If the current through the RTN-to-VSS path is below 29mA, the SY5601A will automatically generate a 2.5V maintain power signature pulsed voltage to the AMPS pin. The current amplitude can be adjusted using an external resistor. When the current through the RTN-to-VSS path exceeds 32mA, the SY5601A exits maintain power signature mode and immediately clears the maintain power signature flag.

Typical Application

Detection Resistor

The input diode bridge's resistance can be hundreds of ohms at low currents. The bridge resistance is in series with R_{DEN} and increases the total resistance seen by the PSE. The resistance varies with the type of diode selected and is not typically specified on the diode datasheet. The value of R_{DEN} may be adjusted downwards to accommodate a particular diode type. A resistor value of 24.9 kΩ ± 1% is recommended for R_{DEN}.

Input Diodes or Diode Bridges

The IEEE 802.3af standard requires the PD to accept power on either set of input pairs and with either polarity. This is achieved using two full-wave input bridge rectifiers, as shown in Figure 1. Silicon p-n diodes with a 1A or 1.5A rating and a minimum breakdown of 100V are recommended. Using Schottky diodes will typically yield to a lower power loss. Diodes exhibit significant dynamic resistance under low-current operating conditions, such as during detection. Therefore, the diodes should be tested for their behavior under these conditions. The total forward drop must be less than 1.5V at 500μA and the lowest operating temperature.

Input Capacitor

During detection, the IEEE 802.3af standard requires a PD input capacitance between 0.05μF and 0.12μF. This capacitor should be placed directly adjacent to the SY5601A, as shown in Figure 1. A 100V, 10%, X7R ceramic capacitor meets the specification over a wide temperature range.

Layout

For optimal power, EMI, and ESD management, the following PCB layout guidelines are recommended:

1. The parts placement must be driven by the power flow point-to-point in this sequence: Ethernet interface, diode bridges, TVS and 0.1-μF capacitor, SY5601A and output capacitor.

2. Keep all leads as short as possible with wide power traces and paired signal and return paths.

3. Position the SY5601A over a local ground plane or fill with copper the PCB area referenced to VSS.

Figures 5 and 6 show the top and bottom layers and assemblies of the SY5601AEVB as a reference for optimal parts placement.

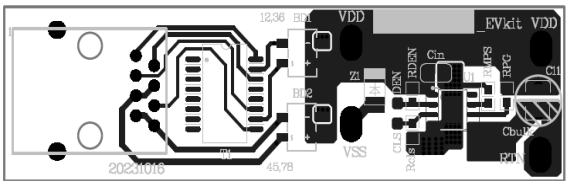


Figure 5. Top Side

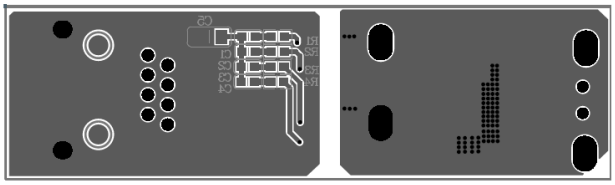


Figure 6. Bottom Side

Typical Application Schematic

This design uses power from the PSE or a 37VDC~57VDC supply. Connect the output to a DC/DC converter with enable control for full verification.

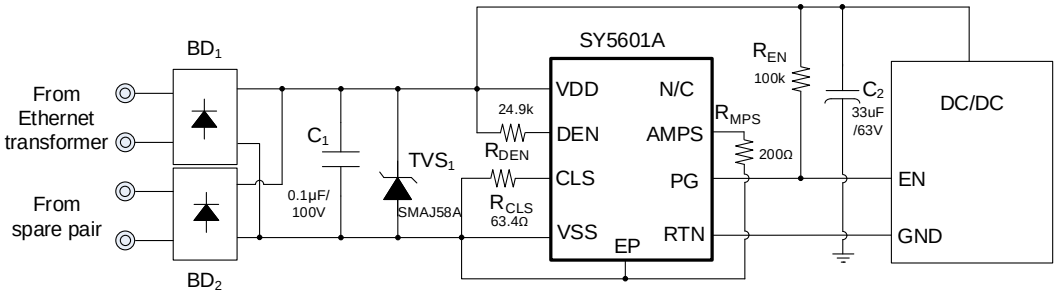
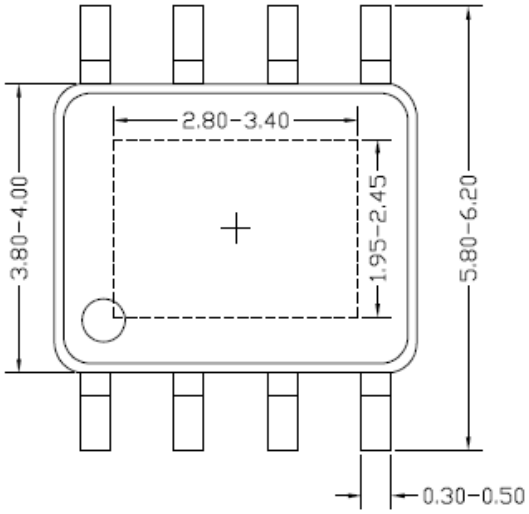


Figure 7. Typical Application Circuit

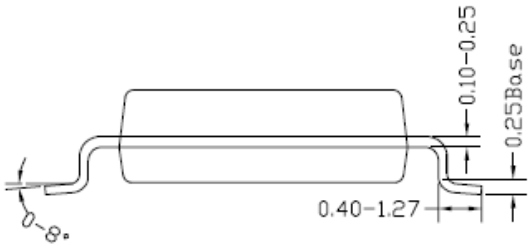
Recommended BOM List

Designator	Description	Part Number	Manufacturer
BD_1,BD_2	0.8A surface mount bridge rectifier	HD01-T	DIODES
C_1	0.1uF/100V,X7R,±10%,0805	AC0603KRX7R0BB104	YAGEO
TVS_1	TVS diode, SMA	SMAJ58A	YANGJIE
R_{DEN}	24.9k, ±1%,0603	RC0603FR-0724K9L	YAGEO
R_{CLS}	63.4, ±1%,0603	AC0603FR-0763R4L	YAGEO
R_{MPS}	180, ±1%,0603	RC0603FR-07180RL	YAGEO
R_{EN}	100k, ±1%,0603	RC0603FR-07100KL	YAGEO
U_1	IEEE 802.3 af/at PoE-Compliant Powered Device (PD) Controller	SY5601A	SILERGY CORP.
C_2	33μF/63V ,Electrolytic capacitor, 6.3x12mm	ERS1JM330E12OT	AIHUA

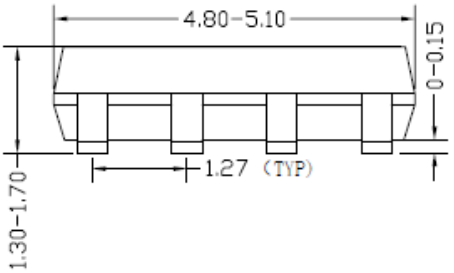
SO8E Package Outline & PCB Layout



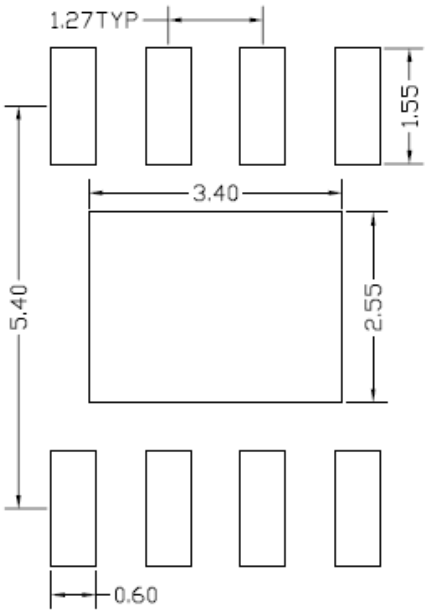
Top View



Side View



Front View

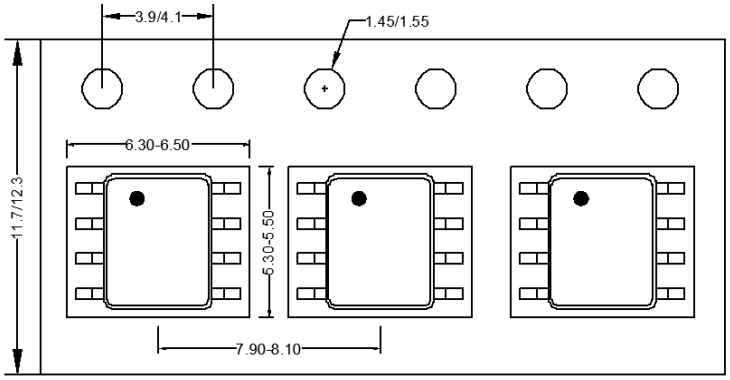


Recommended PCB Layout
(Reference Only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

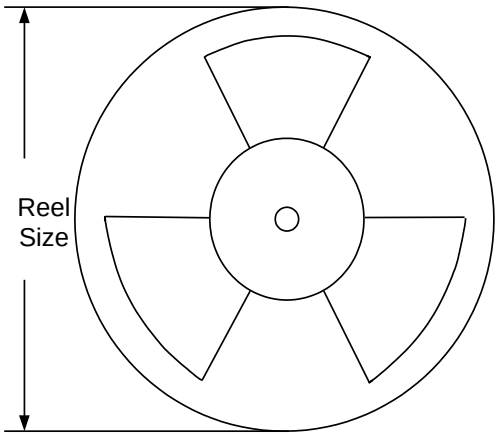
Tape and Reel Specification

SO8E Tape Orientation



Feeding direction ⟶

Carrier Tape and Reel Specification



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SO8E	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
June 25, 2024	Revision 1.0	Initial Release

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