SY5600A

Flyback Controller
With Primary Side CV/CC Control For PoE Application

General Description

SY5600A is a single stage Flyback controller with HV start up circuit targeting at Constant Current/Constant Voltage (CC/CV) applications. Both the output current and voltage are sensed on the primary side, eliminating the opto-isolator and the secondary side feedback circuitry, and minimizing the overall system cost.

SY5600A adopts the quasi-resonant operation and the adaptive PWM/PFM control to achieve the highest average efficiency and the best EMI performance.

SY5600A provides reliable protections including VCC Over Voltage Protection, Short Circuit Protection (SCP), Over Temperature Protection (OTP), Output voltage OVP protection (OVP), and VSEN pin short protection.

Features

- Tight Primary Side CV/CC Regulation
- HV Start-up Circuit Integrated
- PWM/PFM Control for Higher Average Efficiency
- Internal CC/CV Loop Compensation
- Maximum Switching Frequency Limitation 200kHz
- Driver Source/Sink Current:160mA/750mA
- Low Start-up Current: 3μA Maximum
- Reliable Protections for OVP, SCP, OTP
- RoHS Compliant and Halogen Free
- Compact Package: SO8

Applications

- PoE Powered Devices
- DC/DC Convertors
- Security Cameras
- Telecom Systems

Ordering Information

SY5600 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY5600AFAC	SO8	----

Typical Applications

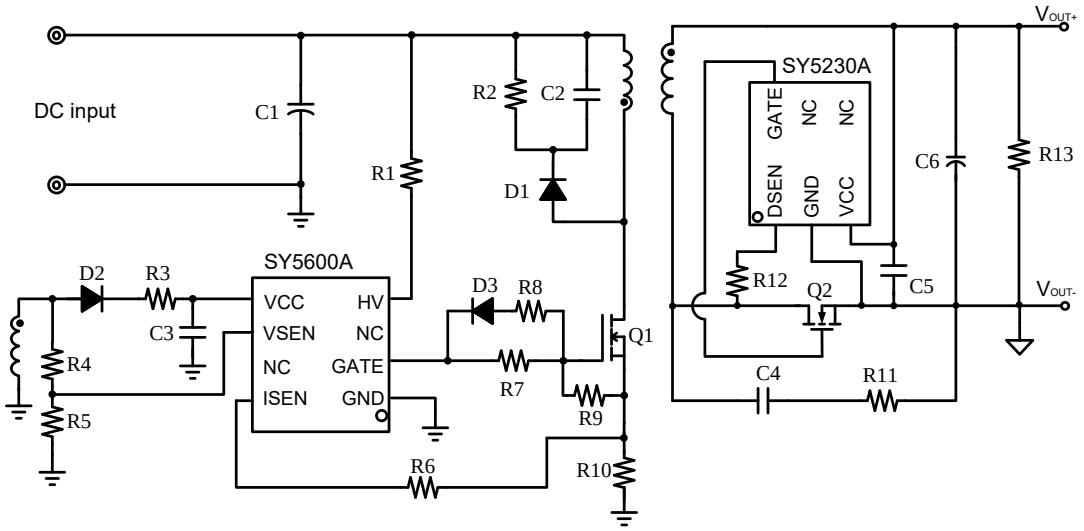
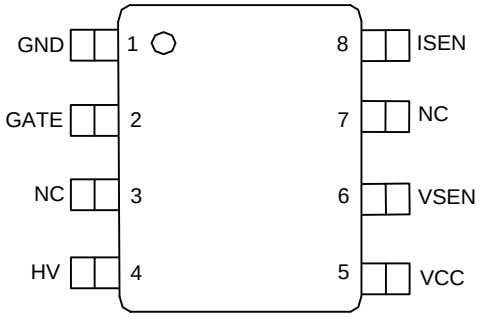


Fig.1 Schematic Diagram

Pinout (top view)



(SO8)

Top Mark: CQB*xyz* (device code: CQB, ***x=year code, y=week code, z= lot number code*****)**

Pin	Name	Description
1	GND	Ground pin.
2	GATE	Gate driver pin. Connect this pin to the gate of primary side MOSFET.
3	NC	Not connect.
4	HV	HV start-up pin. Connect this pin to the BUS directly or through a limited resistor.
5	VCC	Power supply pin.
6	VSEN	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage by a resistor divider and detects the inductor current zero crossing point.
7	NC	Not connect.
8	ISEN	Current sense pin. Connect this pin to the source of the primary side MOSFET.

Absolute Maximum Ratings (Note 1)

VCC---------- -0.3V~21V
ISEN----------0.3V~3.6V
VSEN---------- -0.3V~V_{VCC}+0.3V
HV---------- 700V
Power Dissipation, @ TA = 25°C SO8 ---------- 1.1W
Package Thermal Resistance (Note 2)
SO8, θ_{JA} ---------- 125°C/W
SO8, θ_{JC} ---------- 60°C/W
Junction Temperature Range ---------- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

VCC------- ----------8.5V~15.4V
ISEN---------- 0V~1V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 105°C

Block Diagram

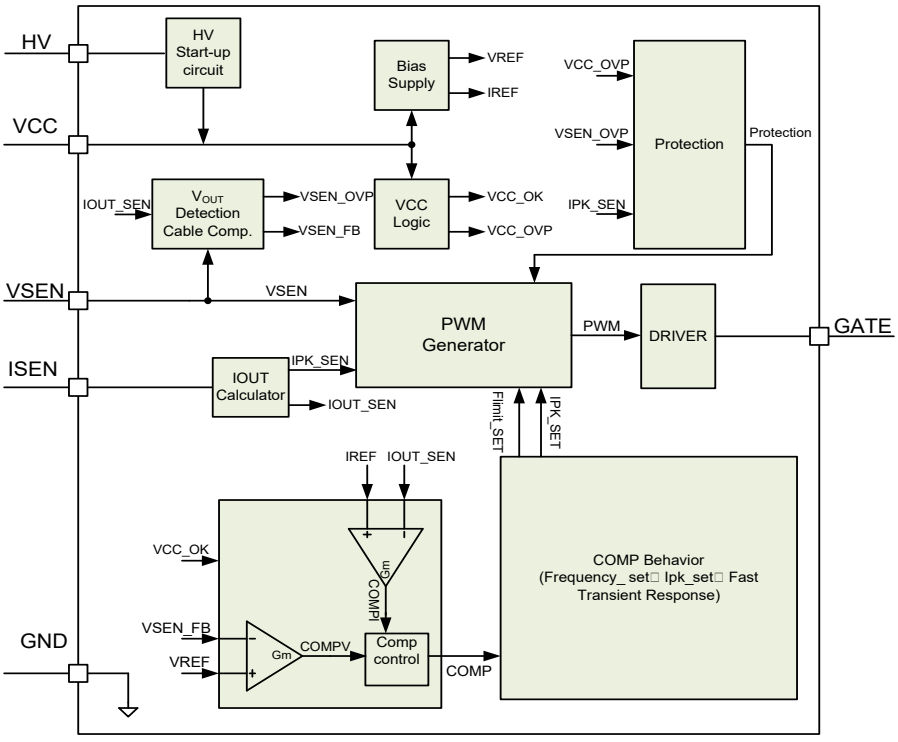


Fig.2 Block Diagram

Electrical Characteristics

(VCC = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VCC Turn-on Threshold	V_{VCC_ON}		8.5	9.5	10.5	V
VCC Turn-off Threshold	V_{VCC_OFF}		6.9	7.7	8.5	V
VCC OVP Voltage	V_{VCC_OVP}			18.2		V
Start up Current	I_{ST}	$V_{VCC}<V_{VCC\_ON}$		1.5	3	μA
Quiescent Current	I_Q	F=2kHz	200	350	500	μA
Discharge Current in OVP Mode	I_{VCC_OVP}			5.2		mA
Current Feedback Modulator Section						
Internal Reference Voltage for Output Current	V_{REF}		0.412	0.420	0.428	V
ISEN Pin Section						
Current Limit Voltage	V_{ISEN_LIM}		0.9	1	1.1	V
VSEN Pin Section						
VSEN Pin OVP Voltage Threshold	V_{VSEN_OVP}		1.38	1.46	1.54	V
Internal Reference Voltage	V_{VSEN_REF}		1.231	1.250	1.269	V
Gate Driver Section						
Gate Driver Voltage	V_{GATE}			12		V
Maximum Source Current	I_{SOURCE_MAX}			160		mA
Maximum Sink Current	I_{SINK_MAX}			750		mA
Max ON Time	T_{ON_MAX}			20		μs
Min ON Time	T_{ON_MIN}			200		ns
Max OFF Time	T_{OFF_MAX}			525		μs
Min OFF Time	T_{OFF_MIN}			600		ns
Minimum Switching Period	T_{SMIN}		3.8	4.5	5.2	μs
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Temperature Hysteresis	T_{SD_HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause perm anent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

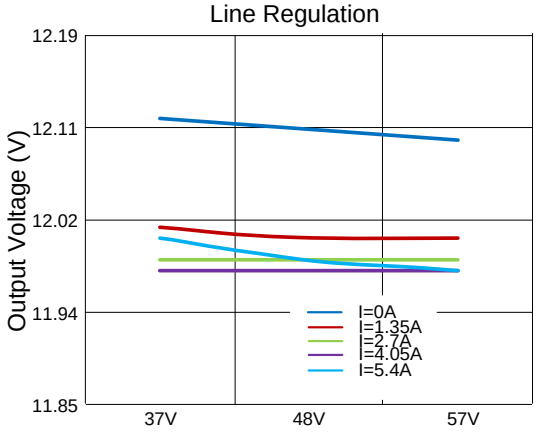
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on "2 x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VCC pin voltage gradually higher than V_{VCC_ON} voltage then regulated to 12V.

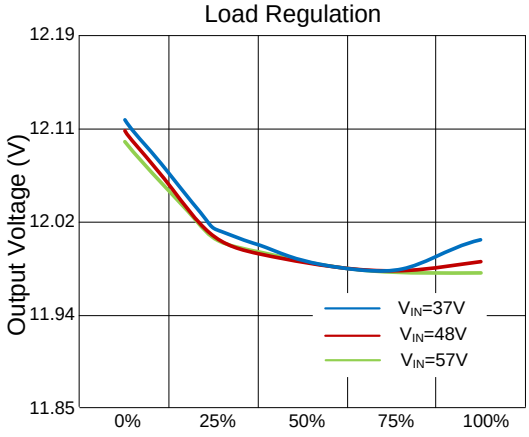
Typical Performance Characteristics

(**Test condition:** input voltage:37~57V_{dc}; output spec:12V_{dc}@5.4A; Ambient temperature: 25±5 ℃ ;Ambient humidity:65±25%.)

Line Regulation

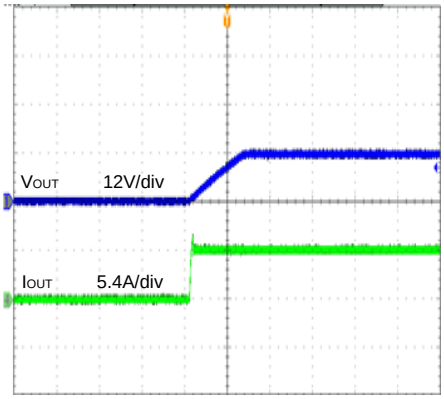


Load Regulation



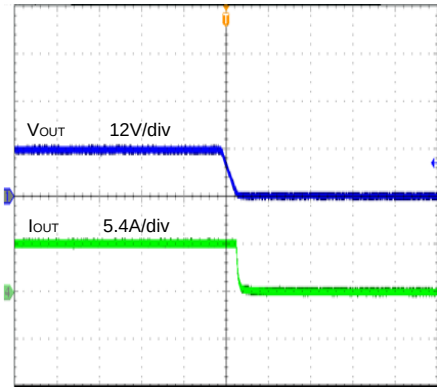
Startup

(V_{IN}=48$V_{(DC)}$)



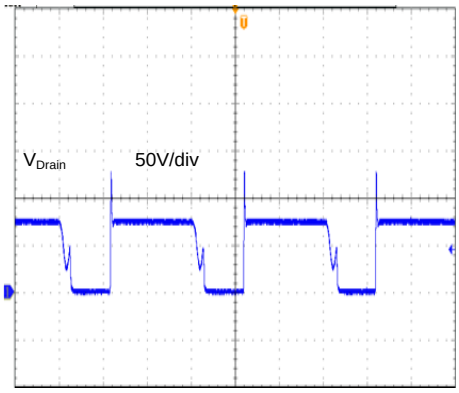
Shutdown

(V_{IN}=48$V_{(DC)}$)



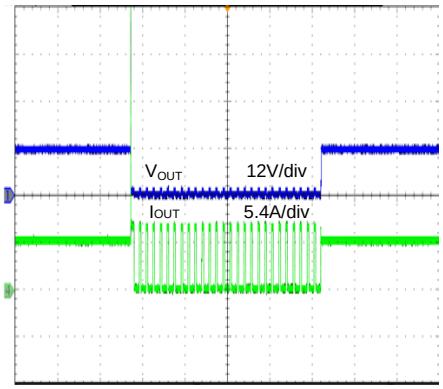
Steady States

(V_{IN}=48$V_{(DC)}$)



Short Circuit Protection

(V_{IN}=48$V_{(DC)}$)



Operation Principles

Start-up Operation

After DC supply is powered on, the rectified BUS voltage ramps up. The capacitor across VCC and GND pins, C_{VCC}, is charged up by the BUS voltage through internal HV start up circuit. Once V_{VCC} rises up to V_{VCC_ON}, the internal blocks starts the operation. V_{VCC} will subsequently be pulled down by the power consumption of the circuitry until the auxiliary winding of Flyback transformer can supply sufficient energy to maintain V_{VCC} above V_{VCC_OFF}.

The start-up procedure is divided into two sections, as shown in Fig.3, t_{STC} is the C_{VCC} charged up section, and t_{STO} is the output voltage built-up section. The start up time t_{ST} composes of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

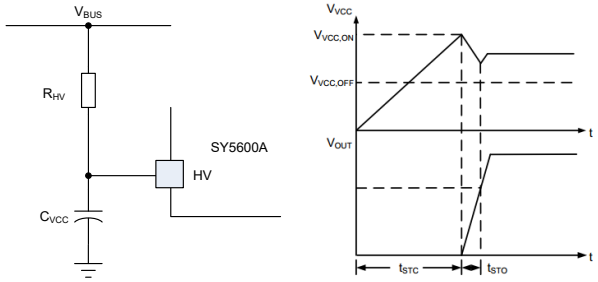


Fig.3 Start up

Shut-down Operation

After DC supply is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer cannot supply enough energy to the VCC pin, V_{VCC} will decrease. Once V_{VCC} is below V_{VCC_OFF}, the IC will stop working.

Quasi-Resonant Operation (Valley Detection)

The Quasi-Resonant switching mode is applied, which means to turn on the integrated MOSFET at voltage valley. QR mode operation provides the low turn-on switching losses for Flyback converter.

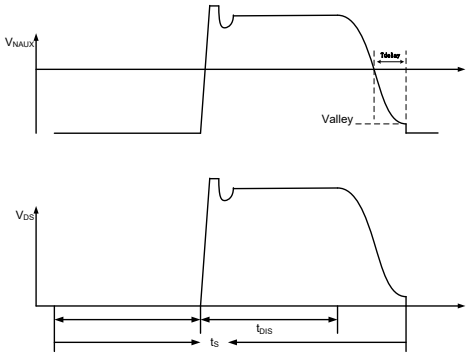


Fig.4 QR mode operation

The voltage across drain and source of the primary integrated MOSFET is reflected to the auxiliary winding of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. As shown in Fig.4, when the voltage on VSEN pin across zero, the MOSFET would be turned on after 400ns delay.

Output Voltage Control (CV Control)

In order to achieve primary side constant voltage control, the output voltage is sensed by the auxiliary winding.

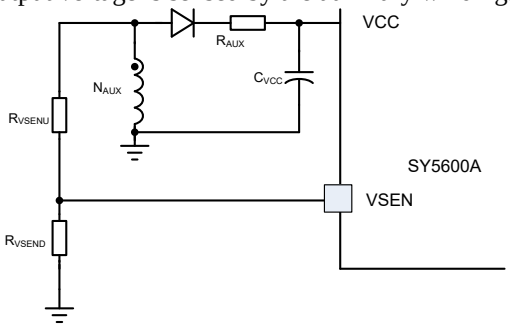


Fig.5 VSEN pin connection

As shown in Fig.6, during off time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D\_F}) \times \frac{N_{AUX}}{N_S} \quad (1)$$

N_{AUX} is the turns of auxiliary winding; N_S is the turns of secondary winding; V_{D_F} is the forward voltage of the secondary side power diode.

At the current zero-crossing point, V_{D_F} is zero, so V_{OUT} is proportional to V_{AUX}. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$\frac{V_{VSEN\_REF}}{V_{OUT}} = \frac{R_{VSEND}}{R_{VSENU} + R_{VSEND}} \times \frac{N_{AUX}}{N_S} \quad (2)$$

where R_{VSEND} and R_{VSENU} are the low side and high resistors at the VSEN pin, respectively, and V_{VSEN_REF} is the internal voltage reference at 1.25V

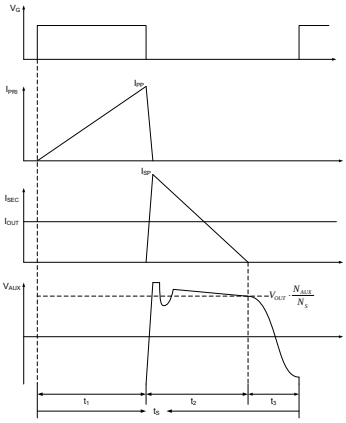


Fig.6 Auxiliary winding voltage waveforms

Output Current Control (CC Control)

The output current is regulated by SY5600A with primary side detection technology, the maximum output current I_{OUT_LIM} can be set by

$$I_{OUT\_LIM} = \frac{k_1 \times V_{REF} \times N_{PS}}{R_S} \quad (3)$$

Where k_1 is the output current weight coefficient; V_{REF} is the internal reference voltage; R_S is the current sense resistor.

k_1 and V_{REF} are all internal constant parameters, I_{OUT_LIM} can be programmed by N_{PS} and R_S.

$$R_S = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT\_LIM}} \quad (4)$$

k_1 is set to 0.5

When the over current operation or short circuit operation takes place, the output current will be limited at I_{OUT_LIM}. The V-I curve is shown as Fig.7.

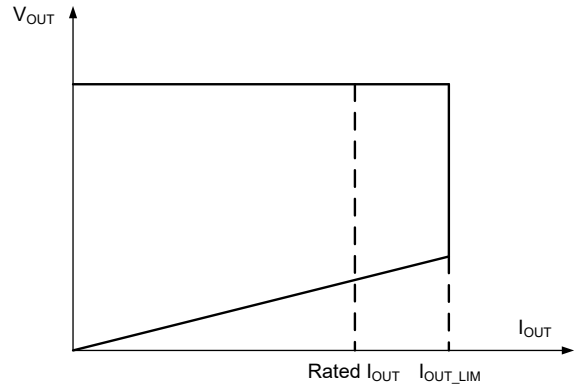


Fig.7 V-I curve

The IC provides line regulation modification function to improve line regulation performance of the output current limit.

Fault Protection modes

VSEN Pin Short Protection

The SY5600A has a protection against the faults caused by a shorted VSEN pin or a shorted pull-down resistor. During start-up, the voltage on the VSEN pin is monitored. In normal situations, the voltage on the VSEN pin reaches the sense protection trigger level. When the VSEN voltage does not reach this level, the VSEN pin is shorted and the protection is activated. The IC stops switching and discharge the VCC voltage. Once V_{VCC} is below V_{VCC_OFF}, the IC will shut down and be charged again by HV start up.

ISEN Pin Short Protection

The SY5600A has a protection against the fault caused by shorting ISEN pin to GND. During start-up, the voltage on the ISEN pin is monitored. If the V_{ISEN} does not exceed 150mV after 2.5μS, the protection will be triggered, the IC stops switching and discharge the VCC voltage. Once V_{VCC} decreases below V_{VCC_OFF}, the IC will shut down and the VCC will be charged again by HV.

Output Over Voltage Protection

When the VSEN pin signal exceeds 1.45V, reflecting an output over-voltage conditions, SY5600A will stop switching and discharge the VCC voltage. Once V_{VCC} is below V_{VCC_OFF}, the IC will shut down and the VCC will be charged again by HV.

VCC Over Voltage Protection

When the VCC voltage exceeds V_{VCC_OVP} threshold, SY5600A will stop switching and discharge the VCC voltage. Once V_{VCC} is below V_{VCC_OFF}, the SY5600A will shut down.

Output Short Circuit Protection (SCP)

There are two kinds of situations, one is the valley signal cannot be detected by VSEN, the other is the valley signal can be detected by VSEN. When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so valley signal cannot be detected by VSEN. There are two cases, the one is without valley detection, MOSFET cannot be turned on until maximum off time is reached. If MOSFET is turned on with maximum off-time for 64 times continuously which can

not detected valley, IC will be shut down and enter into hiccup mode. The other is that IC will be shut down and enter into hiccup mode when V_{VCC} below V_{VCC_OFF} within 64 times. When the output voltage is not low enough to disable valley detection in short condition, SY5600A will operate in CC mode until VCC is below V_{VCC_OFF}. In order to guarantee SCP function not effected by voltage spike of auxiliary winding, a filter resistor R_{AUX} is needed.

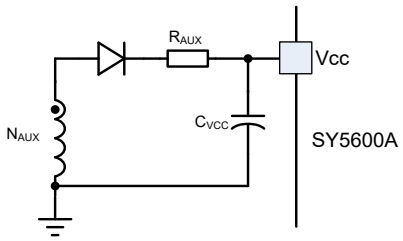


Fig. 8 Filter resistor R_{AUX}

Over-temperature Protection (OTP)

SY5600A includes over-temperature protection (OTP) circuitry to prevent the overheating due to the excessive power dissipation. It will shut down the switching operation when the junction temperature exceeds the OTP threshold, about 150°C. In OTP mode, if the junction temperature decreases by approximately 20°C, the IC will resume the normal operation. For a continuous normal operation, provide an adequate cooling so that the junction temperature does not exceed the OTP threshold.

Power Supply Design Considerations

Transformer Design Considerations (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the internal power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - V_{DC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (5)$$

where $V_{MOS\_(BR)DS}$ is the breakdown voltage of the integrated MOSFET. V_{D_F} is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during off time.

In Quasi-Resonant mode, each switching period cycle, t_S, consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.9.

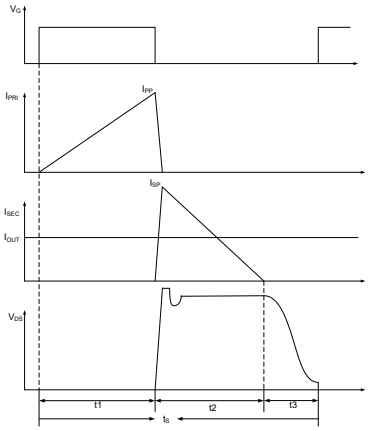


Fig.9 switching waveforms

Under the conditions of the minimum input DC voltage and full load, the switching frequency is minimum while the peak current through integrated MOSFET is maximum.

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be designed. The design flow is shown below:

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - V_{DC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (6)$$

(b) Preset minimum frequency f_{S_MIN}

(c) Compute inductor L_M and maximum primary peak current $I_{P\_PK\_MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times V_{DC\_MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}} \quad (7)$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}} \quad (8)$$

where C_{Drain} is the parasitic capacitance at drain of integrated MOSFET, η is the efficiency, and P_{OUT} is the rated full load power

(d) Compute current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{DC\_MIN}} \quad (9)$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} \quad (10)$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} \quad (11)$$

$$t_S = t_1 + t_2 + t_3 \quad (12)$$

(e) Compute primary maximum RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_S}} \quad (13)$$

(f) Compute secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (14)$$

$$I_{S\_RMS\_MAX} = \frac{\sqrt{3}}{3} N_{PS} \times I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_S}} \quad (15)$$

Transformer Design Considerations

The key transformer parameters are shown below:

Necessary parameters	
Primary to Secondary Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\_PK\_MAX}$
Primary maximum RMS current	$I_{P\_RMS\_MAX}$
Secondary maximum RMS current	$I_{S\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.28T

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} \quad (16)$$

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}} \quad (17)$$

(e) Compute auxiliary turn N_{AUX}

$$N_{AUX} = N_S \times \frac{V_{VCC}}{V_{OUT}} \quad (18)$$

where V_{VCC} is the working voltage of VCC pin (11V~15V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\_RMS\_MAX}$ and $I_{S\_RMS\_MAX}$, select appropriate wire to achieve the current density from 4A/mm^2 to 10A/mm^2.

(g) If the window area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

RCD Snubber for MOSFET Selection

The power loss of the snubber P_{RCD} is evaluated as:

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (19)$$

where V_{OUT} is the output voltage, V_{D_F} is the forward voltage of the power diode, ΔV_S is the overshoot voltage clamped by RCD snubber, L_K is the leakage inductor, L_M is the inductance of the Flyback transformer and P_{OUT} is the output power.

The R_{RCD} is calculated as:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}} \quad (20)$$

The C_{RCD} is calculated as:

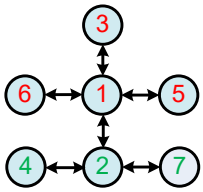
$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} \times f_S \times \Delta V_{C\_RCD}} \quad (21)$$

Layout Considerations

A proper PCB design must follow the below guidelines:
(a) To achieve a good EMI performance and to reduce the line frequency voltage ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

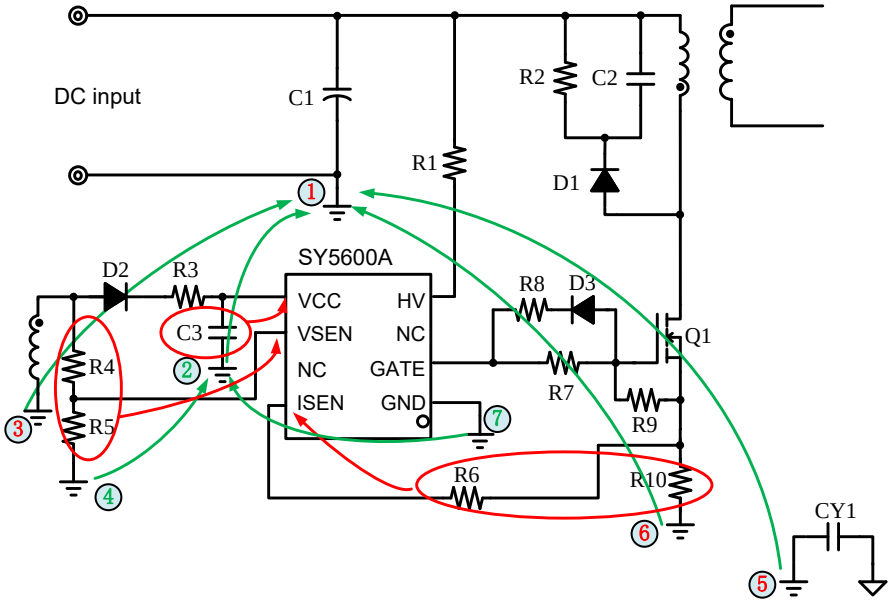
(b) The circuit loop of all switching circuit should be kept as small as possible: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:



Ground ①: ground of BUS line capacitor
Ground ②: ground of bias supply capacitor
Ground ③: ground node of auxiliary winding
Ground ④: ground node of divider resistor
Ground ⑤: primary ground node of Y capacitor
Ground ⑥: ground node of current sample resistor.
Ground ⑦: ground of IC GND.

(d) Bias supply trace should be connected to the bias supply capacitor first and then to the GND pin. The bias supply capacitor should be put right beside the IC.
(e) The loop consisting of ‘Source pin – current sense resistor – GND pin’ should be kept as small as possible.
(f) The resistor divider connected to VSEN pin is recommended to be put close to the IC.



Note□ Ground node of current sample resistor must be connected to the ground of bus line capacitor

Design Notes

1. At no load, the secondary side diode freewheeling time should be more than 0.6us(typical).
2. VCC voltage is recommended to be designed to higher than 11V for all conditions.
3. RCD snubber's influence:
   At no load or light load, the off-time of main switch is very long and the snubber capacitor's voltage may be discharged to a small value. When the primary switch turns on and then turns off, the primary winding current needs a longer than normal time to charge up the snubber capacitor. This might affect the feedback voltage sensing. If I_{min} (I_{min}=0.15V/Rs) is 0.1A, the snubber capacitor should be no larger than 470pF.
4. At heavy load, the peak-to-peak voltage at the VSEN pin should be less than approximately 100mV_{p-p} after off-min time (0.6us,typical). This can be guaranteed by decreasing the leakage inductance and using proper RCD snubber.
5. R_{VSENU} is the upper resistor of the divider. Normally, its value is recommended between 30kΩ~91kΩ.
6. In order to ensure the CC/CV loop stability, the output capacitor should use the following formula to estimate:
   Cout= 3.7m*Iou t/Vout.
   For example, in the 5V/3.1A output case, Cout=3.7*3.1/5=2.312mF. The output capacitor can choose from 1965uF to 2660uF. On the other hand, switching frequency ripple should also be considered. If the switching frequency ripple is too large, increase the capacitance of Cout properly or use low ESR capacitor.

Design Example

A design example of typical application is shown below step by step.
Note: All selected parameter (set value) need to adjust according to the practical condition.

#1. Identify design specification

Design Specification			
V_{DC}	17V~57V	V_{OUT}	12V
I_{OUT}	5.4A	η	85%

#2. Transformer design (N_{PS}, L_M, N_P, N_S, N_{AUX})

(1)Refer to Transformer selection (N_{PS} and L_M)

Conditions			
V_{DC_MIN}	17V	V_{DC_MAX}	57V
ΔV_S	50V	$V_{MOS\_(BR)DS}$	150V
P_{OUT_MAX}	65W	V_{D_F}	1V
C_{Drain}	100pF	f_{S_MIN}	70kHz

(a) Compute turns ratio N_{PS} first:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - V_{DC\_MAX} - \Delta V_S}{V_{OUT} + V_{D,F}}$$

$$= \frac{150V \times 0.9 - 57V - 50V}{12V + 1V}$$

$$= 2.153$$

N_{PS} is set to: $N_{PS} = 2$

(b)f_{S_MIN} is preset

$$f_{S\_MIN} = 70kHz$$

(c) Compute inductor L_M and maximum primary peak current $I_{P,PK,MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times V_{DC\_MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}}$$

$$= \frac{2 \times 65W}{85\% \times 17V} + \frac{2 \times 65W}{85\% \times 2 \times (12V + 1V)} + 3.14 \times \sqrt{\frac{2 \times 65W}{85\%} \times 100pF \times 70kHz}$$

$$= 8.997A + 5.882A + 0.103A$$

$$= 14.982A$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}}$$

$$= \frac{2 \times 65W}{85\% \times (14.982A)^2 \times 70KHz \times 1.05}$$

$$= 9.27 \times 10^{-6} H$$

$$= 9.27uH$$

Set: L_M=9μH

(d) Compute current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{DC\_MIN}} = \frac{9\mu H \times 14.982A}{17V} = 7.931\mu s$$

$$t_2 = \frac{L_m \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} = \frac{9\mu H \times 14.982A}{2 \times (12V + 1V)} = 5.186\mu s$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} = \pi \times \sqrt{17\mu H \times 100pF} = 0.094\mu s$$

$$t_S = t_1 + t_2 + t_3 = 7.931\mu s + 5.186\mu s + 0.094\mu s = 13.21\mu s$$

(e) Compute primary maximum RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_S}} = \frac{\sqrt{3}}{3} \times 14.982A \times \sqrt{\frac{7.931\mu s}{13.21\mu s}} = 6.702A$$

(f) Compute secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2 \times 14.982A = 29.964A$$

$$I_{S\_RMS\_MAX} = N_{PS} \times \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_S}} = 2 \times \frac{\sqrt{3}}{3} \times 14.982A \times \sqrt{\frac{5.186\mu s}{13.21\mu s}} = 10.839A$$

(2)Refer to Transformer number of turnsselection (N_P, N_S, N_{AUX})

(a) Select the magnetic core style, identify the effective area A_e.There select thickened PQ2020 for compute example. Its $A_e$is 62mm^2.The thickened PQ2020 can be replaced by other reasonable magnetic core style.

(b) Preset the maximum magnetic flux ΔB. Usually ΔB=0.22~0.28T .

Set: ΔB=0.270T .

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} = \frac{9*10^{-6}H*14.982A}{0.270T*62*10^{-6}m^2} = 8.055$$

Set: N_P=8

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}} = \frac{8}{2} = 4$$

Set: N_S=4

(e) Compute auxiliary turn N_{AUX}

$$N_{AUX}=N_S\times\frac{V_{VCC}}{V_{OUT}}=4*\frac{12}{12}=4$$

Set: N_{AUX}=4

Where V_{VCC} is the working voltage of VCC pin (11V~15V is recommended).

(f) Select an appropriate wire diameter
With $I_{P\_RMS\_MAX}$ and $I_{S\_RMS\_MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

Primary wire diameter selection:current density j is set to 10A/mm^2.

The compute primary wirecross-sectional area $S1=\frac{I_{P\_RMS\_MAX}}{j}=\frac{6.702}{10}=0.6702mm^2$

The compute primary wire diameter $D1\_1=2*\sqrt{\frac{S1/2}{\pi}}=2*\sqrt{\frac{0.6702/2}{\pi}}=0.653mm$

Set: D1=D1_1*2=0.6mm*2.

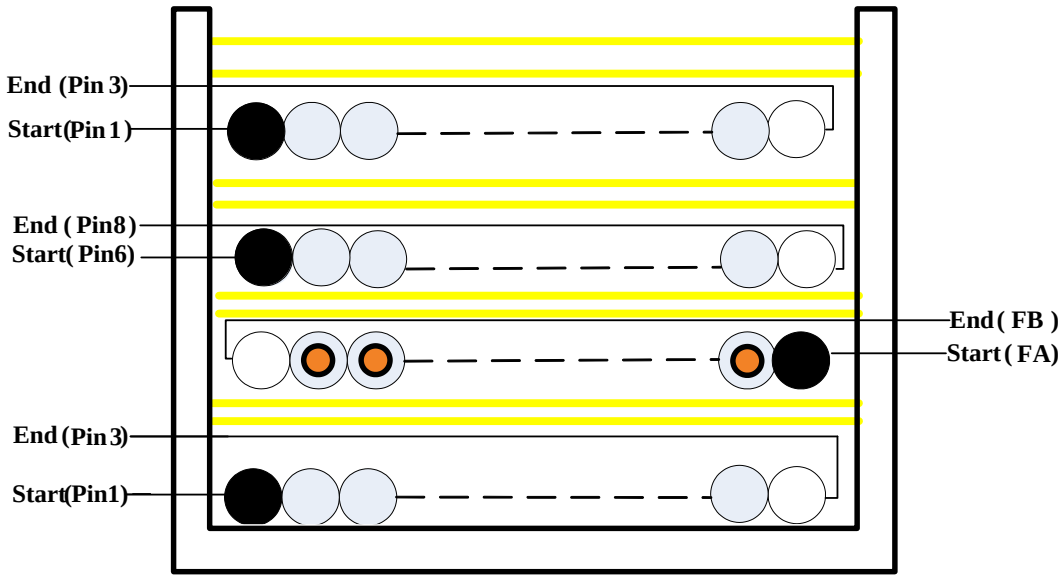
Secondary wire diameter selection:current density j is set to 10A/mm^2.

The compute secondary wirecross-sectional area $S2=\frac{I_{S\_RMS\_MAX}}{j}=\frac{10.839}{10}=1.084mm^2$

The compute secondary wire diameter $D2\_1=2*\sqrt{\frac{S2/4}{\pi}}=2*\sqrt{\frac{1.084/4}{\pi}}=0.588mm$

Set: D2=D2_1*4=0.6mm*4.

Core: thickened PQ2020 PC40
Bobbin: thickened PQ2020 (6+8 pins) Horizontal type



Transformer number parameters

Winding	Wire diameter*Number	Pin		TS	Insulating Tape (TS)	Notes
		IN	OUT			
N1	Φ0.6*2(2UEW)	1	3	8	2	close winding (1 layer)
N2	Φ0.6*4(2UEW)	FA	FB	4	2	close winding (1 layer)
N3	Φ0.2*2(2UEW)	6	8	4	2	Uniform sparse winding (1 layer)
N4	Φ0.6*2(2UEW)	1	3	8	2	close winding (1 layer)

Consider transformer style, the actual primary and secondary wire diameter can be adjusted for best production.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

#3. Select secondary power diode

Refer to Power Device Design

Known conditions at this step			
V_{DC_MAX}	57V	N_{PS}	2
V_{OUT}	12V	V_{D_F}	1V

Compute the voltage and the current stress of secondary power diode

$$V_{D\_R\_MAX} = \frac{V_{DC\_MAX}}{N_{PS}} + V_{OUT}$$
$$= \frac{57V}{2} + 12V$$
$$= 40.5V$$

$$I_{D\_PK\_MAX} = I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2 \times 14.982A = 29.964A$$

$$I_{D\_AVG} = I_{OUT} = 5.4A$$

#4. Set current sense resistor to achieve ideal output current

Known conditions at this step			
N_{PS}	2		
V_{REF_MAX}	1V	I_{OUT_LIM}	7.0A

The current sense resistor is

$$R_S = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT\_LIM}}$$
$$= \frac{0.5 \times 0.42V \times 2}{7.0A}$$
$$= 0.06\Omega$$

Set Rs

R_S=0.05Ω

#5. Set VSEN pin

Refer to V_{OUT}

First identify R_{VSENU} need for line regulation.

Parameters Designed			
R_{VSEND}	15kΩ		

Then compute R_{VSENU}

Conditions			
V_{OUT}	12V	V_{VSEN_REF}	1.25V
R_{VSEND}	15kΩ	N_S	4
N_{AUX}	4		

$$R_{VSENU} = R_{VSEND} \times \left(\frac{V_{OUT} N_{AUX}}{V_{VSEN\_REF} N_S} \text{-} 1 \right) = 15k \times \left(\frac{12V \times 4}{1.25V \times 4} - 1 \right) = 129k$$

Set R_{VSENU}

R_{VSENU} =150k Ω//680k Ω

#6. Final result

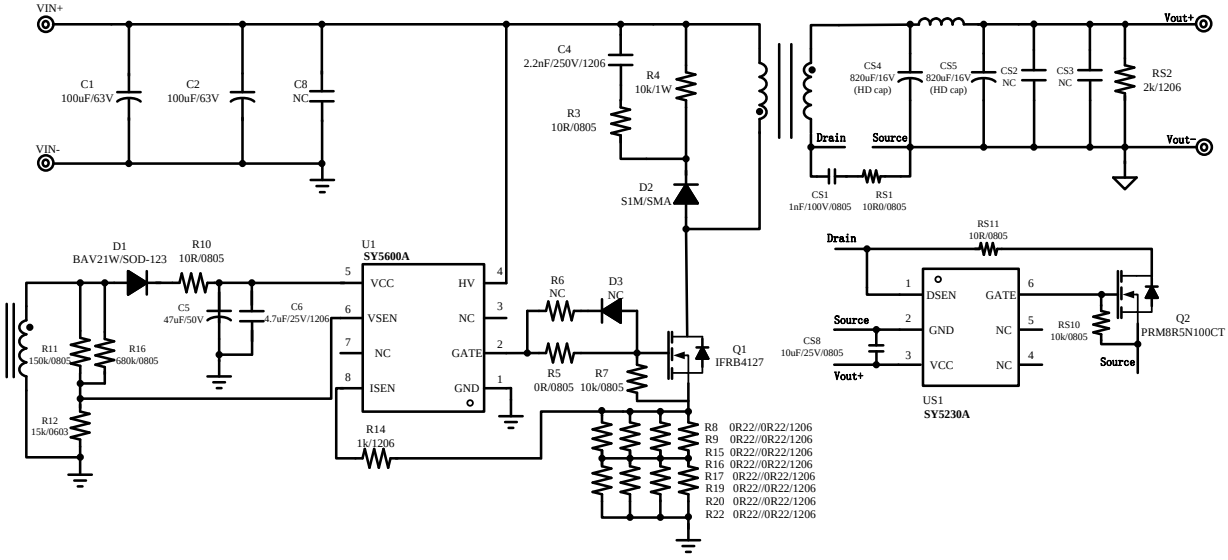
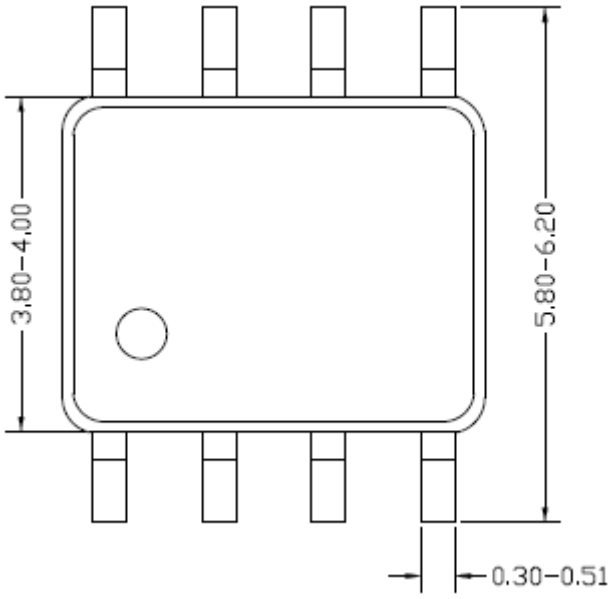
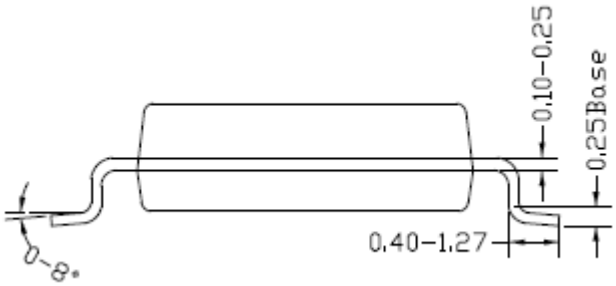


Fig.10 Final Schematic of the SY5600A 65W Design Example
(V_{IN}: 17VDC~57VDC, V_{OUT}=12V, I_{OUT_MAX}=5.4A)

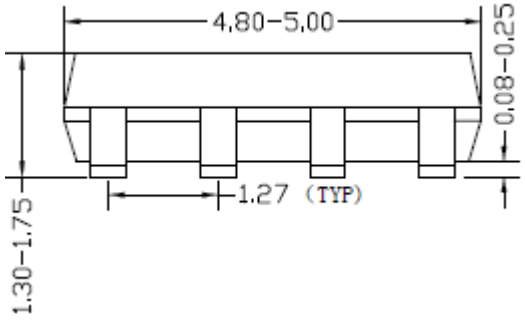
SO8 Package outline & PCB layout design



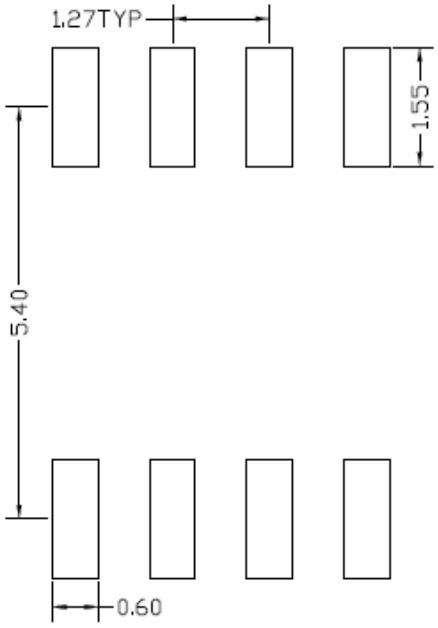
Top view



Side view



Front view

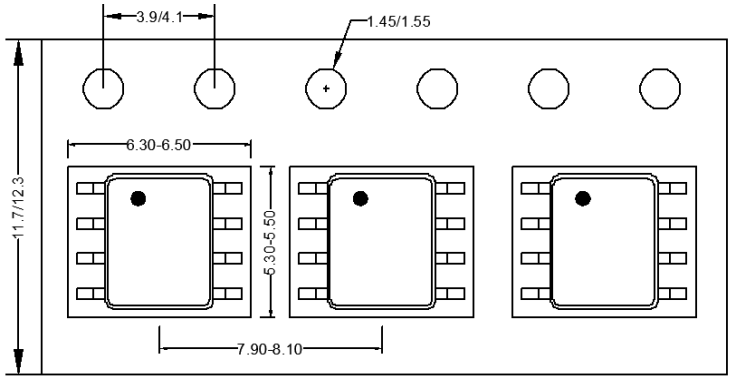


Recommended Pad Layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

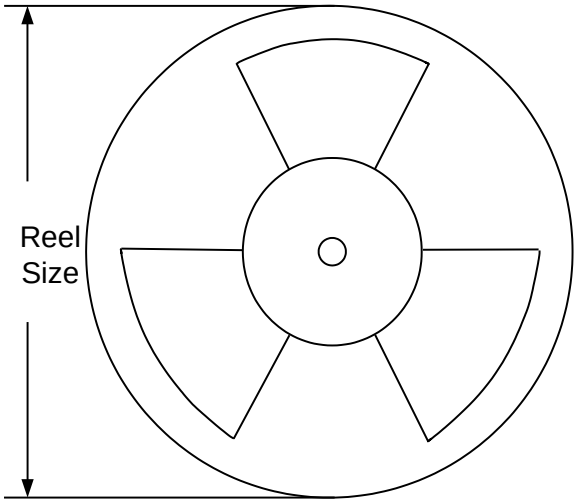
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
July 10, 2019	Revision 0.9	Initial Release

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