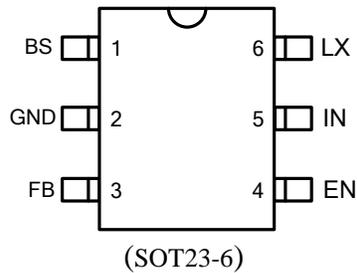


Pinout (top view)


Top Mark: TExyz (Device code: TE, *x*=year code, *y*=week code, *z*= lot number code)

| Pin Name | Pin Number | Pin Description |
|----------|------------|--|
| BS | 1 | Boot-Strap Pin. Supply high side gate driver. Decouple this pin to LX pin with 0.1uF ceramic cap. |
| GND | 2 | Ground pin. |
| FB | 3 | Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6 \times (1+R1/R2)$. |
| EN | 4 | Enable control. Pull high to turn on. Do not float. |
| IN | 5 | Input pin. Decouple this pin to GND pin with at least 1uF ceramic cap. |
| LX | 6 | Inductor pin. Connect this pin to the switching node of inductor. |

Absolute Maximum Ratings (Note 1)

| | |
|---|--------------------------|
| Supply Input Voltage | -0.3V to 42V |
| Enable Voltage | -0.3V to $V_{IN} + 0.6V$ |
| FB Voltage | -0.3V to 3.6V |
| BS to LX Voltage | -0.3V to 3.6V |
| LX voltage | -0.7V to $V_{IN}+0.6V$ |
| Power Dissipation, P_D @ $T_A = 25^\circ C$, SOT23-6 | 0.6W |
| Package Thermal Resistance (Note 2) | |
| θ_{JA} | 170°C/W |
| θ_{JC} | 130°C/W |
| Junction Temperature Range | -40°C to 150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Storage Temperature Range | -65°C to 150°C |
| Dynamic LX voltage in 10ns duration | -IN+3V to GND-5V |

Recommended Operating Conditions (Note 3)

| | |
|----------------------------|----------------|
| Supply Input Voltage | 5V to 40V |
| BS to LX Voltage | 3.3V |
| Junction Temperature Range | -40°C to 125°C |
| Ambient Temperature Range | -40°C to 85°C |

Electrical Characteristics

($V_{IN} = 20V$, $V_{OUT} = 12V$, $L=22\mu H$, $C_{OUT} = 4.7\mu F$, $T_A = 25^\circ C$, $I_{OUT} = 100mA$ unless otherwise specified)

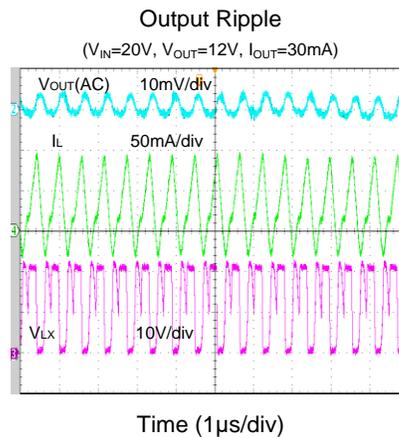
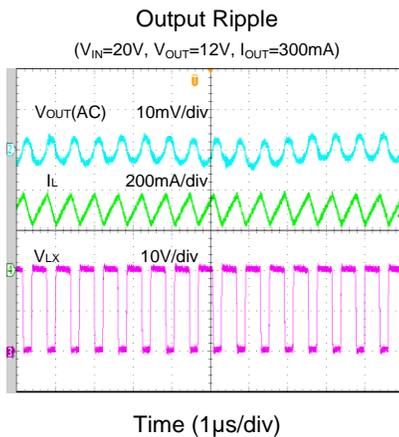
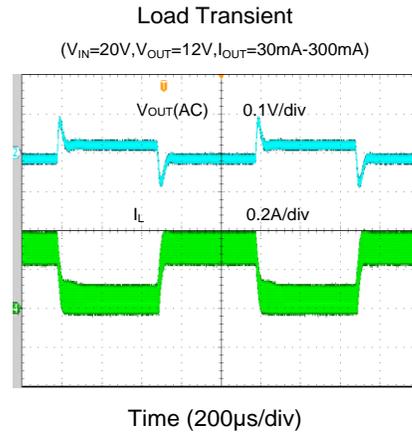
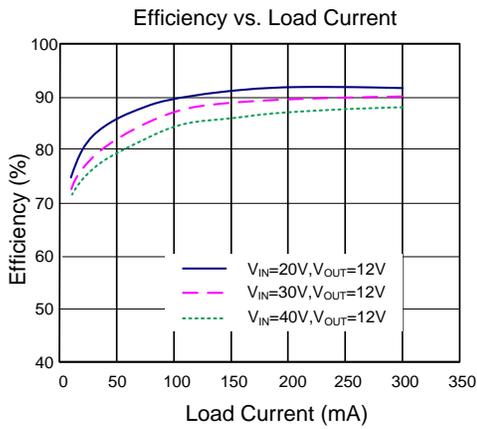
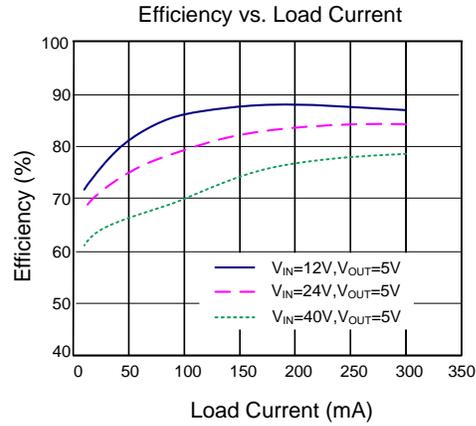
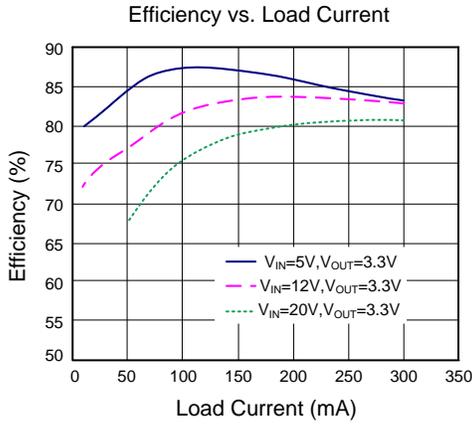
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|------------------------------|-----------------|--|-------|-----|-------|------------|
| Input Voltage Range | V_{IN} | | 5 | | 40 | V |
| Input UVLO Threshold | V_{UVLO} | Rising | | 4.5 | | V |
| Input UVLO Hysteresis | V_{UVLO_HYS} | | | 200 | | mV |
| Quiescent Current | I_Q | $I_{OUT}=0$, $V_{FB}=V_{REF}\times 105\%$ | | 160 | | μA |
| Shutdown Current | I_{SHDN} | EN=0 | | | 10 | μA |
| Feedback Reference Voltage | V_{REF} | | 0.588 | 0.6 | 0.612 | V |
| FB Input Current | I_{FB} | $V_{FB}=V_{IN}$ | -50 | 10 | 50 | nA |
| Power FET RON | $R_{DS(ON)1}$ | | | 2 | | Ω |
| Power FET Current Limit | I_{LIM} | | 450 | | | mA |
| EN Rising Threshold | V_{ENH} | | 1.5 | | | V |
| EN Falling Threshold | V_{ENL} | | | | 0.4 | V |
| Minimum OFF Time | t_{OFF} | | | | 100 | ns |
| Minimum ON Time | t_{OFF} | | | | 100 | ns |
| Soft Start Time | t_{SS} | | | 400 | | us |
| Switching Frequency | F_{SW} | | 1.6 | 2 | 2.4 | MHz |
| Thermal Shutdown Temperature | T_{SD} | | | 150 | | $^\circ C$ |
| Thermal Recovery Hysteresis | T_{HYS} | | | 15 | | $^\circ C$ |

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θJ_A is measured in the natural convection at $T_A = 25^\circ C$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

Typical Performance Characteristics



Startup From VIN

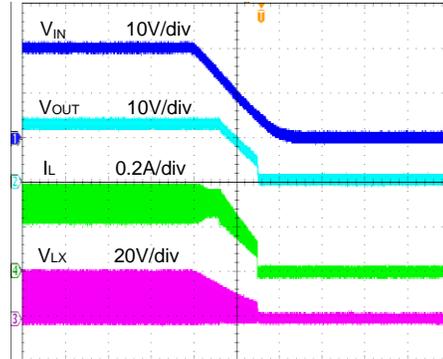
($V_{IN}=20V$, $V_{OUT}=12V$, $I_{OUT}=300mA$)



Time (4ms/div)

Shutdown From VIN

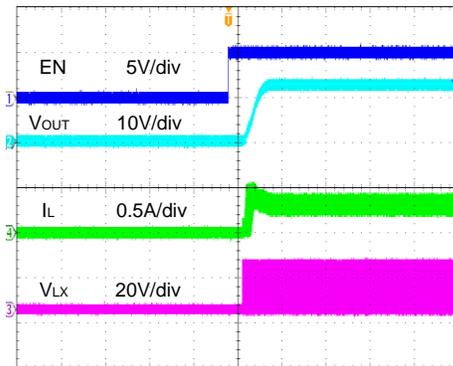
($V_{IN}=20V$, $V_{OUT}=12V$, $I_{OUT}=300mA$)



Time (20ms/div)

Startup From Enable

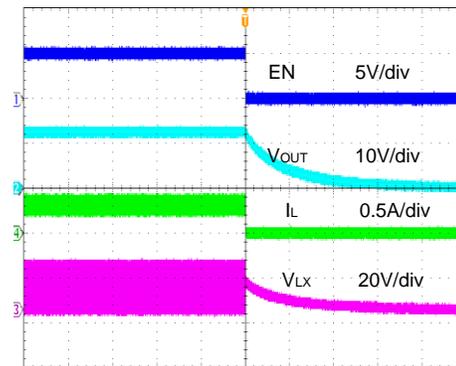
($V_{IN}=20V$, $V_{OUT}=12V$, $I_{OUT}=300mA$)



Time (800 μ s/div)

Shutdown From Enable

($V_{IN}=20V$, $V_{OUT}=12V$, $I_{OUT}=300mA$)



Time (200 μ s/div)

Operation

SY8290 is an asynchronous buck regulator IC that integrates the PWM control, main switch on the same die. High switch frequency minimizes the external inductor and capacitor size, thus minimizes the PCB area and cost. It features low output voltage ripple, cycle by cycle current limit, output short circuit protection and thermal shutdown protection.

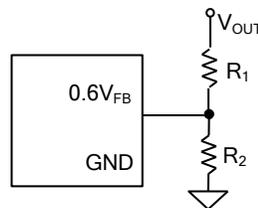
Applications Information

Because of the high integration in the SY8290 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN} , output capacitor C_{OUT} , output inductor L rectifier diode and feedback resistors (R_1 and R_2) need to be selected for the targeted applications.

Feedback resistor dividers R_1 and R_2 :

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2 . A value of between $10k\Omega$ and $1M\Omega$ is highly recommended for both resistors. If V_{out} is 5V, $R_1=100k$ is chosen, then using following equation, R_2 can be calculated to be 13.7k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1$$



Input capacitor C_{IN} :

The ripple current through input capacitor is calculated as:

$$I_{CIN_RMS} = I_{OUT} \cdot \sqrt{D(1-D)}$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN pin and the negative end of rectifier. A low ESR ceramic capacitor is recommended with greater than $1\mu F$ capacitance.

Output capacitor C_{OUT} :

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with greater than $4.7\mu F$ capacitance.

Output inductor L :

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY8290 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

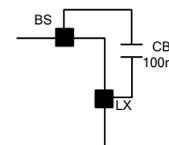
- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT, MIN} > I_{OUT, MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with $DCR < 50m\Omega$ to achieve a good overall efficiency.

External Bootstrap Cap

This capacitor provides the gate driver voltage for internal high side MOSEFET. A $100nF$ low ESR ceramic capacitor connected between BS pin and LX pin is recommended.

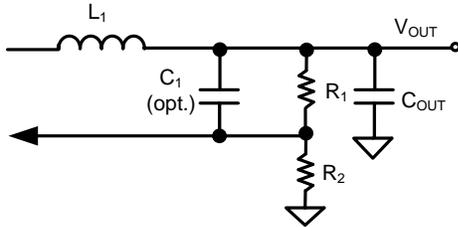


Rectifier Diode

Because of high switching speed of SY8290, a schottky diode with low forward voltage and fast switching speed is desirable for the application. The voltage rating of the diode must be higher than maximum output voltage. The diode's average and peak current rating should exceed the average output current and peak current.

Load Transient Considerations:

The SY8290 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a small ceramic cap in parallel with R1 may further speed up the load transient response and is it is recommended for high step load applications.



Layout Design:

The layout design of SY8290 regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC: C_{IN} , L, R1 and R2.

- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- 2) The loop area formed by IN, LX, C_{IN} and the rectifier diode must be minimized.
- 3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
- 4) The components R_1 and R_2 , and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.
- 5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

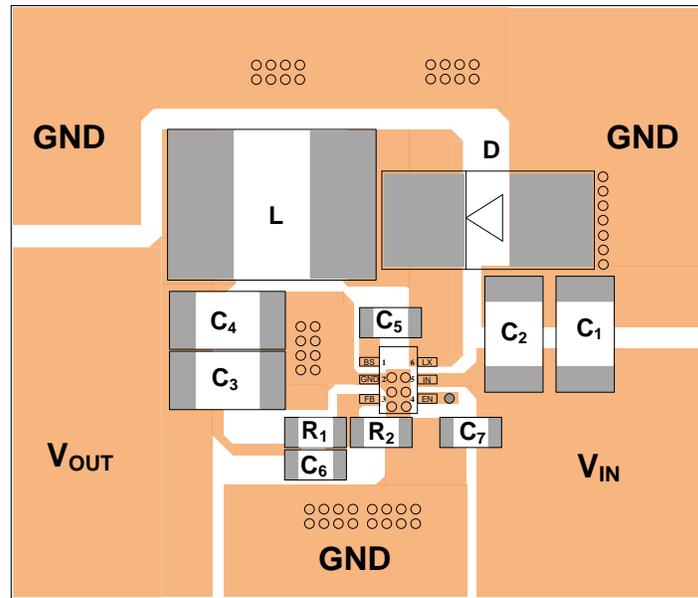
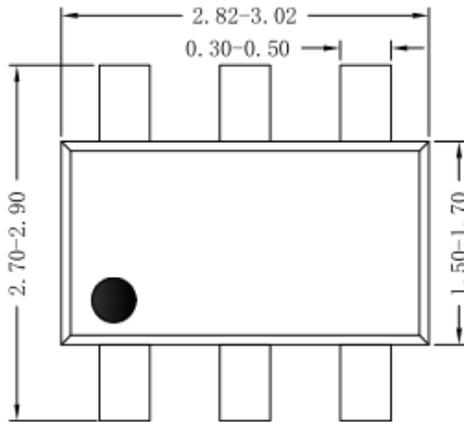
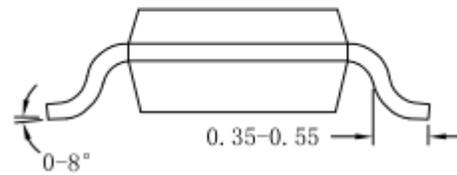


Figure 3. PCB Layout Suggestion

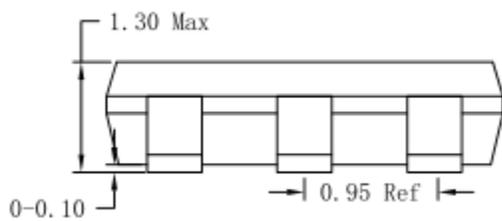
SOT23-6L Package Outline & PCB Layout



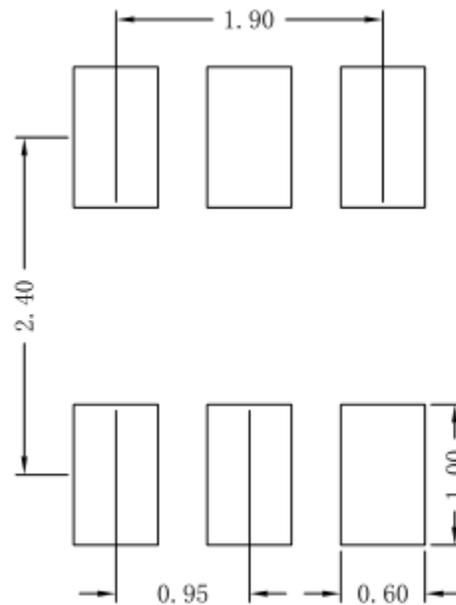
Top View



Side View



Side View

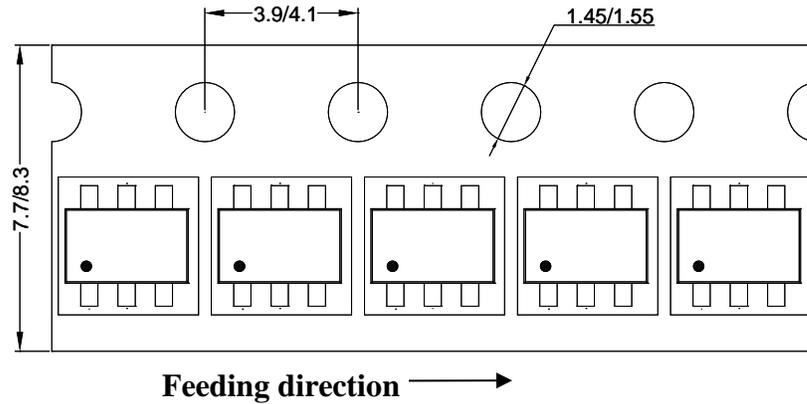


Recommended Pad Layout

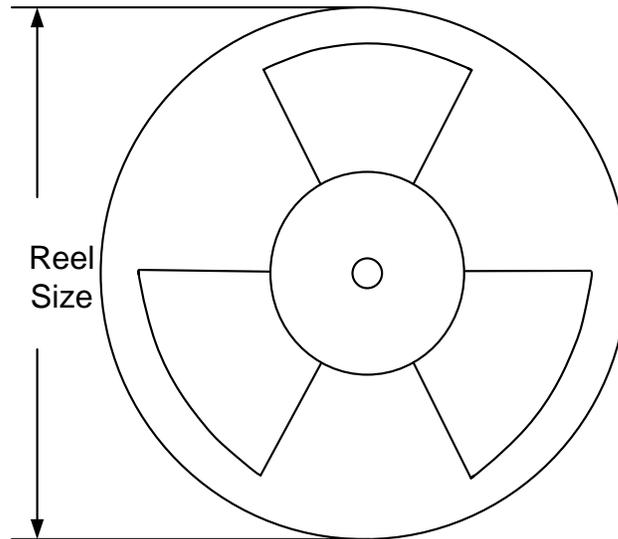
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

1. Taping orientation



2. Carrier Tape & Reel specification for packages



| Package types | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|---------------|-----------------|------------------|------------------|--------------------|--------------------|--------------|
| SOT23-6 | 8 | 4 | 7" | 280 | 160 | 3000 |

3. Others: NA

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